國立中山大學109學年度
碩士暨碩士專班招生考試試題

科目名稱：計算機結構【電機系碩士班己組】

—作答注意事項—

考試時間：100分鐘

- **考試開始鈴響前不得翻閱試題，並不得書寫、劃記、作答。**請先檢查答案卷（卡）之應考證號碼、桌角號碼、應試科目是否正確，如有不同立即請監試人員處理。
- **答案卷限用藍、黑色筆(含鉛筆)書寫、繪圖或標示**，可攜帶橡皮擦、無色透明無文字墊板、尺規、修正液（帶）、手錶(未附計算器者)。每人每節限使用一份答案卷，不得另攜帶紙張，請衡酌作答。
- 答案卡請以2B鉛筆劃記，不可使用修正液（帶）塗改，未使用2B鉛筆、劃記太輕或污損致光學閱讀機無法辨識答案者，其後果由考生自行負擔。
- 答案卷（卡）應保持清潔完整，不得折疊、破壞或塗改應考證號碼及條碼，亦不得書寫考生姓名、應考證號碼或與答案無關之任何文字或符號。
- 可否使用計算機請依試題資訊內標註為準，如「可以」使用，廠牌、功能不拘，唯不得攜帶具有通訊、記憶或收發等功能或其他有礙試場安寧、考試公平之各類器材、物品（如鬧鈴、行動電話、電子字典等）入場。
- **試題及答案卷（卡）請務必繳回，未繳回者該科成績以零分計算。**
- **試題採雙面列印，考生應注意試題頁數確實作答。**
- **違規者依本校招生考試試場規則及違規處理辦法處理。**

國立中山大學109學年度碩士暨碩士專班招生考試試題

科目名稱：計算機結構【電機系碩士班己組】　　題號：431007

※本科目依簡章規定「可以」使用計算機（廠牌、功能不拘）（問答申論題）　　

1. [20%] (1) (8%) Add one-sentence comments to each of the following MIPS code to describe what it computes. (2) (12%) Write the C code that corresponds to the following MIPS code. Assume that registers $a1 and $a2 stores the base address of arrays A and B, and the register $t1 stores the value of a variable i.

```
li $t1, 0

for: lw $s1, $s1($a1)

     beq $s1 0, end
     lw $s2, $s1($a2)

     add $s1, $s2, $s1
     add $s1, $s1, $t1

     addi $t1, $s0, 1

     bne $t1 20, for
end:
```

2. [20%] Explain the following terms.

(a) (4%) Amdahl's law
(b) (4%) Data hazard
(c) (4%) Exceptions
(d) (4%) Flush
(e) (4%) Spatial locality

3. [20%] Give answers to the following questions.

(a) (4%) Given a single precision IEEE 754 bit stream S: 1011 1110 1110 0000 0000 0000 0000 0000. What does this floating number mean? Write your final answer with decimal expression.
(b) (8%) Draw the flow chart of floating-point addition. Also explain how the floating-point addition is performed by using this flow chart.
(c) (8%) Design a hardware unit that can perform floating-point addition. Please draw the block diagram of your designed hardware unit and explain how this hardware works.

4. [20%] The following questions are for the five-pipeline-stage MIPS processor design.

(a) (5%) What are the contained pipeline stages and their tasks to be executed?
(b) (9%) Draw the **data path** of the five-pipeline-stage MIPS processor
(c) (6%) For the lw instruction, which control signals are needed and how are these control signals transferred with pipeline operations for the data path you drew in (b)?

5. [20%] Cache memory

(a) (4%) What are direct-mapped cache, set-associative cache and fully associative cache?
(b) (6%) Draw the architecture of a four-way set-associative cache that contains totally 16 blocks.
(c) (6%) Draw the flow chart of the cache architecture you drew in (b) and explain how the cache works with this flow chart.
(d) (4%)What is the "write-through" scheme? What is the possible problem with this scheme and how can we solve the problem?