編號: 121

國立成功大學 109 學年度碩士班招生考試試題

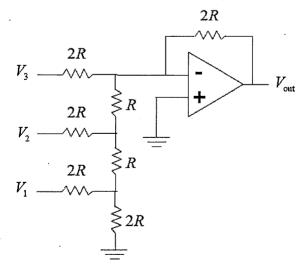
系 所:工程科學系 考試科目:電子電路

考試日期:0211, 節次:1

第1頁,共3頁

※ 考生請注意:本試題可使用計算機。 請於答案卷(卡)作答,於本試題紙上作答者,不予計分。

- 1. Mark each of the following statements True (T) or False (F). (Need NOT give reasons.) (20 pt.)
 - (a) Provided that the power supplied by the power plant is the same, while the supplied voltage changes from 350000 V to 175000 V. Assuming that the transmission line obeys the Ohm's law, the power dissipated in the transmission line reduces to a factor of 0.25.
 - (b) The small signal model of a Zener diode in the breakdown region is a DC voltage plus a resistor.
 - (c) The large signal model of a typical diode in the forward region can be approximated as a DC voltage plus a resistor.
 - (d) The input currents of ideal amplifiers are 0 because their open-loop gains are infinite.
 - (e) Typical diodes can function in the breakdown region irrespective of the current flowing through it.
 - (f) Differential amplifier can reject the common-mode input under all conditions.
 - (g) Low-pass single-time-constant circuits mean that only signals with low amplitudes can be passed (or amplified) to the output.
 - (h) One of the advantages of a differential amplifier is that DC coupling can be applied in it.
 - (i) Doping intrinsic silicon with impurity atoms like a trivalent element forms n type semiconductor.
 - (j) At room temperature, there are no free electrons and holes in intrinsic silicon.
- 2. (a) Find V_{out} , when $V_1 = V_2 = V_3 = 5 \text{ V}$. (b) Find V_{out} , when $V_1 = V_3 = 5 \text{ V}$ and $V_2 = 0 \text{ V}$. (20 pt.)



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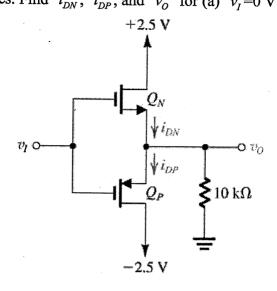
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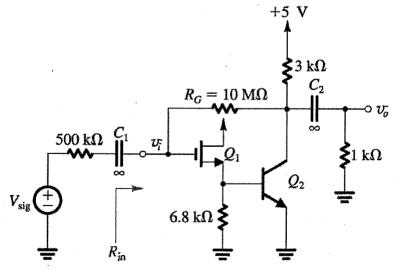
第2頁,共3頁

考試日期:0211,節次:1

3. The NMOS and PMOS transistors are matched with $k_n' \left(\frac{W}{L} \right)_n = k_p' \left(\frac{W}{L} \right)_p = 1 \text{ mA/V}^2$ and $V_{tn} = -V_{tp} = 1 \text{ V}$. Besides, $\lambda = 0$ for both devices. Find i_{DN} , i_{DP} , and v_O for (a) $v_I = 0 \text{ V}$ and (b) +2.5 V. (20 pt.)



- 4. (a) Consider the dc bias. Neglect the base current of Q_2 . Assume the dc bias current in Q_1 is 100 uA, find the dc bias current in Q_2 . (Assume $|V_{BE}| = |V_t| = 0.7 \text{ V}$, $\mu_n Cox(W/L) = 2 \text{ mA/V}^2$)
 - (b) Determine the voltage gain $A_v = v_o/v_i$. For this purpose you can neglect R_G . (20 pt.)



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第3頁,共3頁

5. For the circuit below, find the overall voltage gain v_o/v_i with $g_{m1}=g_{m2}=5$ mA/V and neglect r_o . (20 pt.)

