# 國立成功大學 109 學年度碩士班招生考試試題

系　所：光電科學與工程學系

考試科目：電子學

考試日期：0211，節次：1



※ 考生請注意：本試題不可使用計算機。 請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. Transistor in Fig. 1 has $V_{BE\,(on)} = 0.7$ and $\beta = 100$. $D_1$ is a Schottky diode with turn on voltage of 0.3 V. $D_2$ is a Zener diode with $V_Z = 5.4$ V. Please find the output voltage ($V_{out}$) when input voltage ($V_{in}$) is 6 V. (10%)

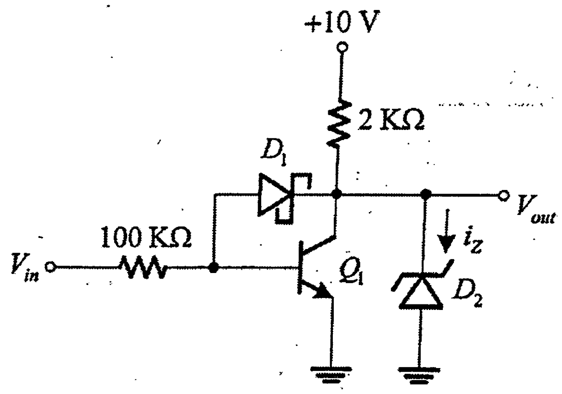


Fig. 1

2. Consider the BiCMOS amplifier shown in Fig. 2. The BJT has $|V_{BE}| = 0.7$ V, $\beta = 200$, $C_\mu = 0.8$ pf, and $f_T = 600$ MHz. The NMOS transistor has $V_t = 1$ V, $K'_n(W/L) = 2$ mA/V$^2$, and $C_{gs} = C_{gd} = 1$ pF. (30%)

(a) Consider the dc bias circuit. Neglect the base current of $Q_2$ in determining the current in $Q_1$. Find the DC bias currents in $Q_1$ and $Q_2$. Evaluate the small signal parameters of $Q_1$ and $Q_2$ at their bias points.

(b) Consider the circuit at mid-band frequencies. First determine the small signal voltage gain $V_o/V_i$. Then use Miller theorem on $R_G$ to determine the amplifier input resistance $R_{in}$. Finally, determine the overall voltage gain $V_o/V_{sig}$.

(c) First consider the circuit at low frequencies. Determine the frequency of poles due to $C_1$ and $C_2$, and hence estimate the lower 3-dB frequency, $f_L$. Second consider the circuit at high frequencies. Use Miller's theorem to replace $R_G$ with a resistance at the input. Use open circuit time constants to estimate $f_H$.

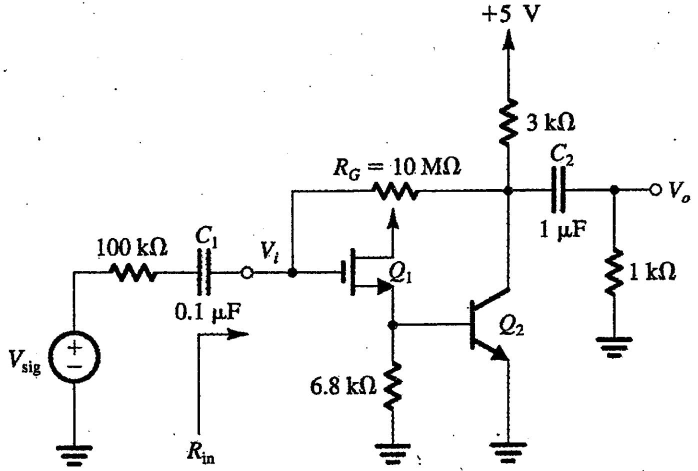


Fig. 2

3. Figure 3 shows a MOS differential amplifier. (30%)

(1) Derive $I_{bias}$ (current flowing through $M_1$) in terms of R, $\mu_n C_{ox}$ and $(W/L)_n$, where $(W/L)_1 = 2(W/L)_n$, $(W/L)_2 = (W/L)_4 = (W/L)_5 = (W/L)_n$, $(W/L)_3 = 4(W/L)_n$, and $(W/L)_6 = (W/L)_7 = (W/L)_p$. Assume $|V_t|$ is the same for all devices.

(2) Derive the small-signal voltage gain $v_o/v_i$.

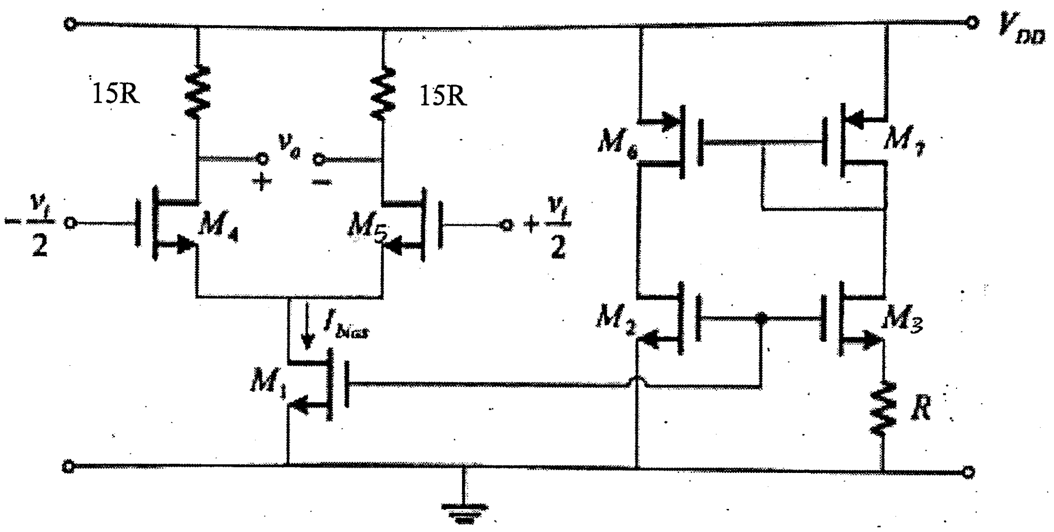


Fig. 3

4. The $V_{DD}$, input DC bias, and $I_{BIAS}$ in Fig. 4 are 5 V, 3 V, and 300 μA, respectively. The transistors in Fig. 4 have $\mu_n C_{ox} W_1/L_1 = \mu_p C_{ox} W_2/L_2 = \mu_p C_{ox} W_3/L_3 = \mu_p C_{ox} W_4/L_4 = 200\ \mu A/V^2$, $V_{tn} = 1$ V, and $V_{tp} = -1$ V. (20%)

(a) What is the output DC voltage of the circuit?

(b) Find the small-signal voltage gain of the circuit.

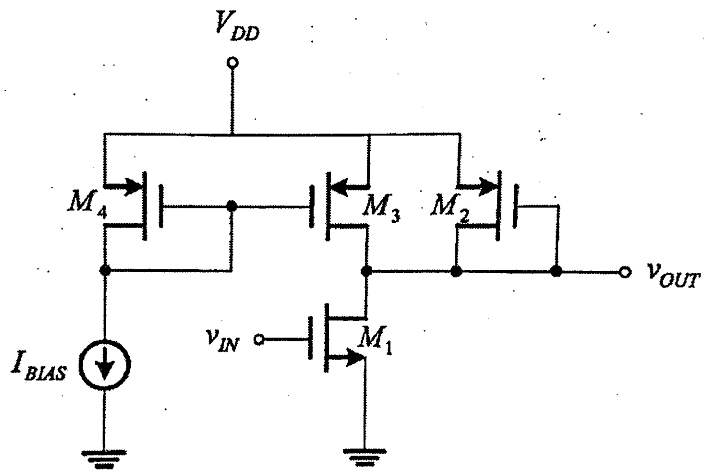


Fig. 4

5. For an ideal BJT the $I_C$ doesn't vary with the $V_{CE}$ when BJT is in active mode. However, each $I_C$-$V_{CE}$ curve in the realistic $I_C$-$V_{CE}$ characteristics of BJT of Fig. 5 shows that the $I_C$ slightly increases with increasing the $V_{CE}$ when BJT is in active. The injected carrier profiles in base region of BJT with different scenarios of bias are showing in Fig. 6. Which figure in Fig. 6 is the cause of slight increases of $I_C$ with enlarged $V_{CE}$ for BJT in active mode? And give your interpretation about the figure you pick in Fig. 6 why it is the cause of slight increases of $I_C$ with enlarged $V_{CE}$ for BJT in active mode. (10%)

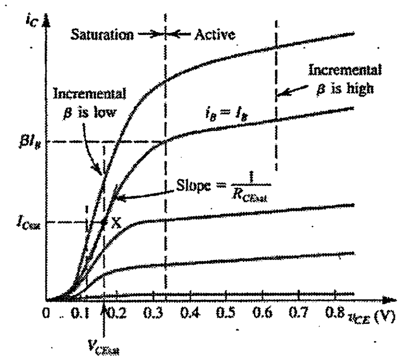


Fig. 5

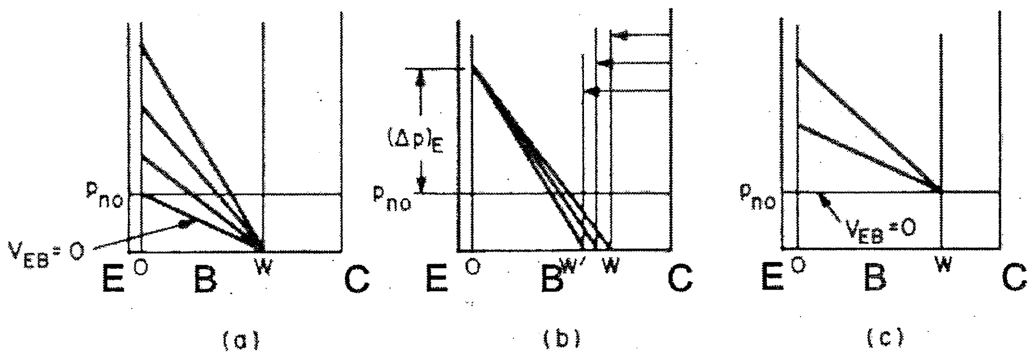


Fig. 6