編號： 170

國立成功大學 109 學年度碩士班招生考試試題

系　　所：電機工程學系

考試科目：計算機組織

考試日期：0210，節次：2

※ 考生請注意：本試題不可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. For a five-stage pipeline processor with L1 ICache and L1 DCache, answer the following questions. (5 points each, 25 points total)

a. Show a simple datapath diagram for PC = PC + 4

b. In the pipelined datapath, what components should be connected to the CPU clock?

c. If a L1 data cache miss occurs, how to handle the pipeline operation?

d. An illegal instruction is detected at which pipeline stage?

e. What is precise interrupt?

2. For stack operations, answer the following questions. (5 points each, 15 points total)

a. What is a callee?

b. What is a stack pointer?

c. What is a jump-and-link instruction?

3. A cache is 128KB in size, and its line size is 32 bytes. The address length is 32 bits. Answer the following questions? (5 points each, 20 points total)

a. If the cache is implemented in direct-mapping, how many cache lines does the cache have?

b. Continued from a., what is the length (bits) of the index field used to select a cache line?

c. If the cache is implemented in 4-way set associative, what is the length (bits) of the index field used to select a cache line?

d. If the cache is implemented in fully set associative, what is the length (bits) of the index field used to select a cache line?

Choose the most appropriate answers for the following multiple choice problems. Each question may have more than one answer. 10 points each, no partial point, no penalty.

4. Which of the following is (are) true for virtual memory system?
   a. Virtual memory function can be enabled through instructions.
   b. Virtual memory technique treats part of the main memory as a fully-set associative write-back cache for program execution.
   c. A translation lookaside buffer (TLB) can be seen as the cache of the virtual memory.
   d. A page table is the data structure used by a virtual memory system in a computer operating system to store the mapping between virtual addresses and physical addresses.

5. Which of the following is (are) true for TLB?
   a. The page offset is part of the address stored in a TLB.
   b. A DTLB (data TLB) is looked up using the address from the program counter.
   c. An ITLB (instruction TLB) is looked up using the address from the program counter.
   d. TLB caches the mapping of virtual pages to physical pages.

6. Which of the following is (are) true when a processor is booted from power-on?
   a. The initial program counter is loaded by the processor from a specified memory location through a load instruction at booting.
   b. The first instruction is fetched using the program counter value specified by operating system.
   c. The BIOS provides the address of the first instruction being fetched.
   d. The initial program counter is preset in the program counter register through hardware operation.

7. Which of the following is (are) true about cache?
   a. Cache is pronounced as [kætʃ].
   b. When a write operation is observed to a location that a cache has a copy of, the cache controller invalidates its own copy of the snooped memory location, which forces a read from main memory of the new value on its next access. This is the write-invalidate cache coherency protocol.
   c. When a cache write miss occurs, the written data are directly updated in the next level of memory. This is the write-around policy.
   d. When a cache write hit occurs, the written data are only updated in the cache without writing to the next level of memory. This is the write-back policy.