國立臺灣科技大學 108 學年度碩士班招生試題

系所組別：電機工程系碩士班丁二組

科　　目：控制系統與數位邏輯

(總分為 100 分)

Problem 1: (15 points) 說明：計算題 15 分，每小題 5 分。

Consider a negative unity-feedback system, $T(s)=\dfrac{L(s)}{1+L(s)}$, with loop transfer function

$L(s)=KG(s)=K(s+1)^3,\ K\in R;$

(a) (5 points) draw the root-locus plot for $0<K<\infty$,

(b) (5 points) draw the root-locus plot for $-\infty<K<0$,

(c) (5 points) determine the range of K such that the close-loop system is stable.

Problem 2: (15 points) 說明：計算題 15 分，每小題 5 分。

Consider a negative unity-feedback system, $T(s)=\dfrac{L(s)}{1+L(s)}$, with loop transfer function

$L(s)=\dfrac{-(s-2)}{(s+1)^2}$;

(a) (5 points) compute the phase crossover frequency ω_{cp} and the gain margin GM,

(b) (5 points) compute the gain crossover frequency ω_{cg} and the phase margin PM,

(c) (5 points) determine that the close-loop system is stable or not?

Problem 3: (10 points) 說明：計算題 10 分，每小題 5 分。

Given a first-order open-loop control system with system input-output transfer function $G(s)=\dfrac{Y(s)}{U(s)}=\dfrac{1}{s+1}$ and initial state $y(0)=y_0$;

(a) (5 points) design a control input signal in the form of $u(t)=\begin{cases}u_0(t) & 0\le t\le T\\ 0 & \text{otherwise}\end{cases}$, such that output $y(T)=0$, where $u_0(t)$ is to be determined,

(b) (5 points) compute the corresponding output response $y(t)$, $t\ge 0$.

Problem 4: (10 points) 說明：計算題 10 分。

Consider a negative unity-feedback system with loop transfer function $L(s)=\dfrac{\omega_n^2}{s(s+2\zeta\omega_n)}$,

where $0<\zeta<1$, $\omega_n>0$, and let $s=-m\omega+j\omega$, where $m,\omega>0$; find m and ω such that

$L(-m\omega+j\omega)=-1$.

國立臺灣科技大學 108 學年度碩士班招生試題

系所組別：電機工程系碩士班丁二組

科　　目：控制系統與數位邏輯

Problem 5: Design a BCD counter using logic gate(s) and 4-bit binary ripple counter in Fig. 1, which counts 0, 1, .., 15, and then goes back to zero to repeat the count. Here A_3 is MSB. **(10 points)**

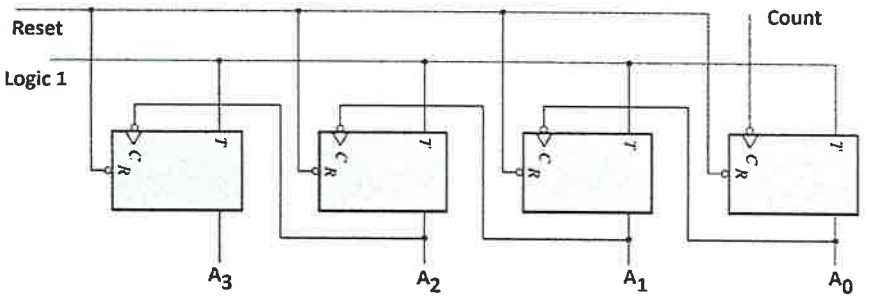

Fig.1. Four-bit binary ripple counter.

Problem 6: (a) Using JK-FF designs a counter with the following repeated binary sequence: **0, 2, 4, 6, 8**. You must present **state table, K-map,** and **logic diagram. (15 points)** (b) What are the responses of **unused states**? Is it a **self-correcting** circuit? **(6 points)**

Problem 7: Consider Four-Bit Universal Shift Register in Fig. 2. Give the following input conditions:

```
initial #300 $finish;
initial begin CLK = 0, forever #5 CLK = ~CLK; end
initial fork
   Clear_b = 0;                          // Power-up initialization
   #20  Clear_b = 1;                     // Running
   In_par = 4'b1010;                     // Word for parallel load; 1010=A
   MSB_in = 1'b1;                        // Bit for serial load
   LSB_in = 1'b0;                        // Bit for serial load
   s1 = 0; s0 = 0;                       // Initial action to no change
   #40  begin s1 = 1; s0 = 1; end        // parallel load
   #60 Clear_b = 1'b0;                   // Reset on-the-fly
   #80 Clear_b = 1'b1;                   // Resume action with parallel load at next clock edge
   #90 begin s1 = 0; s0 = 0; end         // No action – register holds 4'b1010
   #120 Clear_b = 1'b0;                  // Clear register
   #130 Clear_b = 1'b1;
   #140 begin s1 = 1'b0; s0 = 1'b1; end  // Shifting to right (from MSB)
   #170 begin s1 = 1'b0; s0 = 1'b0; end  // Register should hold 4'b1111
   #190 begin Clear_b = 1'b0; s1 = 1'b0; s0 = 1'b0; end
   #200 begin Clear_b = 1'b1; s1 = 1'b1; s0 = 1'b0; end   // Resume action – shift left
   #230 begin s1 = 1'b0; s0 = 1'b0; end
join
```

Plot the input signals, i.e., **CLK, Clear_b, s1,s0, In_par[3:0], (7 points)** and the corresponding output responses, i.e., **A_par [3:0], MSB_in, LSB_in,** y_3, y_2, y_1, y_0 **(12 points)**. Some explanations are suitable.

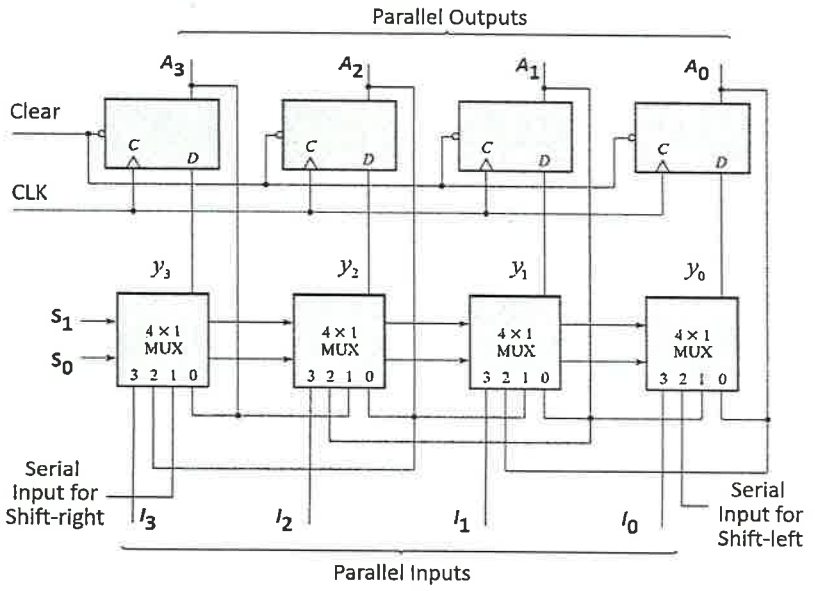

Fig. 2. Four-bit Universal Shift Register.

END