元智大學 108 學年度 碩士班 招生試題卷

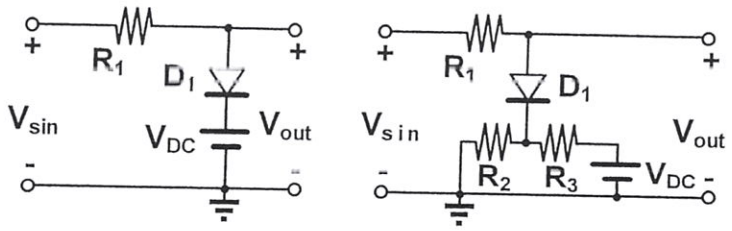
系(所)別：電機工程學系碩士班　組別：甲組　科目：電子學　用紙第 1 頁共 2 頁

●不可使用電子計算機

Problem 1: (15%) (a) For the chopper circuit shown in Fig. 1(a), V_{sin} is a 10-Hz 5-V peak sine wave with zero offset, D_1 is a diode with a constant voltage drop $V_D = 0.7$ V, $R_1 = 1$ kΩ, and $V_{DC} = 1$ V. Use the constant-voltage-drop diode model to draw wavforms V_{in} and V_{out} vesus time with their maximum amplitudes. (7%)

(b) V_{out} is not flat because of the dynamic resistance. Please describe the dynamic resistance. (4%)

(c) For the reconneted chopper circhit shown in Fig. 1(b), V_{sin} is a 10-Hz 5-V peak sine wave with zero offset, D_1 is a diode with a constant voltage drop $V_D = 0.7$ V, $R_1 = R_2 = 1$ kΩ, $R_3 = 2$ kΩ, and $V_{DC} = 3$ V. Use the constant-voltage-drop diode model to draw wavforms V_{in} and V_{out} vesus time with their maximum amplitudes. (4%)



(a)　(b)

Fig. 1

Problem 2: (25%) (a) Please describe the Boolean function of an exclusive-OR gate using an output signal Y and two input signals A and B. (7%)

Using MOSFET transistors,

(b) sketch a static CMOS logic circuit that realizes the exclusive-OR gate (8%),

(c) sketch a dynamic logic circuit that realizes the exclusive-OR gate (5%), and

(d) sketch a pass transistor logic circuit that realizes the exclusive-OR gate. (5%)

Problem 3: (20%) Consider a typical Opamp with two amplification stages (A_{v1} and A_{v2}) and an output buffer stage. The input and output impedance of each stage is denoted as R_{in1}, R_{out1}, R_{in2}, and R_{out2}. A compensation capacitance C_c is placed across A_{v2}. (Assume the input impedance→∞ in the output buffer stage.)

(a) Neglect other parasitic capacitance, and determine the –3dB bandwidth of the Opamp by Miller Effect. (10%)

(b) Redo (a) without using Miller Effect and verify the result is the same as (a). (10%)

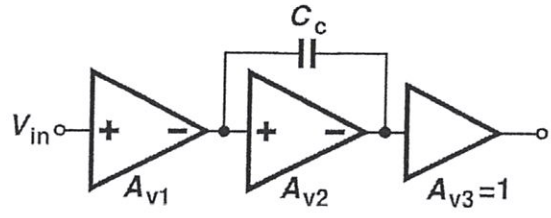


Fig. 2

Problem 4: (40%) Consider the following circuits. Neglect the channel length modulation and Body Effect.

(a) Determine the output impedance of Fig. 3(a) if only C_{gs} is taken into consideration. (10%)

(b) From (a), under what condition does the impedance become inductive? (10%)

(c) Determine the zero in Fig. 3(b) without calculating the transfer function. (10%)

(d) From (c), determine the impedance of the load consisting C_1, R_1, and M_2. (10%)

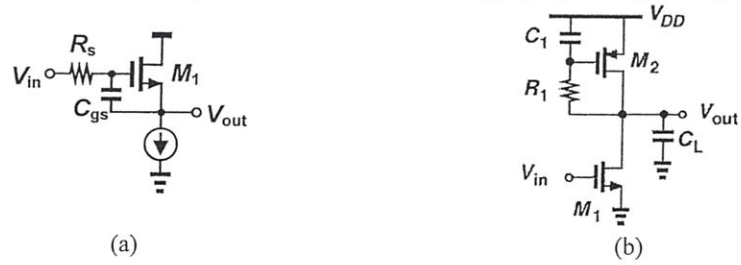


Fig. 3