考試科目	計算机系统	所別	資訊科学	考試時間	3月15日 星期六 第二節

Operating Systems 2008 Master Entrance Examination

There are 10 problems for this examination and the weights for each (sub)problem is indicated. Please do all of them.

1. Please answer the following questions:

   (a) (4%)What is the purpose of system calls?

   (b) (6%)What are three general methods used to pass parameters to the operating system in the system calls during different circumstances?

2. Please answer the following questions:

   (a) (5%) Why we have to guard against race condition and synchronize the critical section?

   (b) (5%)A solution to the critical-section problem must satisfy the following three requirements: mutual exclusion, progress, and bounded waiting. Assume the elements of the array boolean flag[2] are initialized false. Please justify whether the following algorithm for the structure of process P_i where $i = 0, 1$ satisfies these three requirements for two-process synchronization. Your answer must explicitly prove each condition's satisfaction:

```
do {
     flag[i] = true;
     while (flag[j]);

     critical section

     flag[i]=false;

     remainder section
   } while (1);
```

3. (8%) A file is to be shared among different processes, each of which has a unique number. The file can be accessed simultaneously by several processes, subject to the following constraint: The sum of all unique numbers associated with all the processes currently accessing the file must be less than n. Write a monitor to coordinate access to the file.

備考	試題隨卷繳交
命題委員：	（簽章）2008年 3月 5日

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4. (12%) Consider a file currently consisting of 40 blocks. Assume that the file control block (and the index block, in case of indexed allocation) is already in memory. Calculate how many disk I/O operations are required for contiguous, linked, and indexed (single-level) allocation strategies, if, for one block, the following conditions hold. In the contiguous allocation case, assume that there is no room to grow in the beginning, but there is room to grow in the end. Assume that the block information to be added is stored in memory:

   (a) The block is added at the beginning.

   (b) The block is added in the middle.

   (c) The block is removed from the middle.

   (d) The block is removed from the end.

5. Please answer the following questions:

   (a) (5%)Assume we have a demand-paged memory. The page table is held in registers. It takes 15 *ms* to service a page fault if an empty page is available or the replaced page is not modified, and 25 *ms* if the replaced page is modified. Memory access time is 100 *ns*. Assume that the page to be replaced is modified 80 percent of the time. What is the maximum acceptable page-fault rate for an effective access time of no more than 100 *ns*?

   (b) (5%)Consider a demand-paging system with a paging disk that has an average access and transfer time of 10 *ms*. Addresses are translated through a page table in main memory, with an access time of 2 μs per memory access. Thus, each memory reference through the page table takes two accesses. To improve this time, we have added an associated memory that reduces access time to one memory reference, if the page-table entry is in the associative memory.Assume that 80 percent of the accesses are in the associative memory, and that, of the remaining, 20 percent (or 4 percent of the total) cause page faults. What is the effective memory access time?

備考	試題隨卷繳交
命題委員：	（簽章）2018年 3月 5日

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6. **[Multilevel Cache]** Consider 3 processors with different cache configurations:
   - Cache 1: Direct-mapped with one-word blocks
   - Cache 2: Direct-mapped with four-word blocks
   - Cache 3: Two-way set associative with four-word blocks

   The following miss rate measurements have been made:
   - Cache 1: instruction miss rate is 4%; data miss rate is 6%
   - Cache 2: instruction miss rate is 3%; data miss rate is 4.5%
   - Cache 3: instruction miss rate is 2%; data miss rate is 3%

   For these processors, one-third of the instructions contain a data reference. Assume that the cache miss penalty is 8 + Block size in words. The CPI for this workload was measured on a processor with cache 1 and was found to be 2.0. (a) Determine which processors spend the most cycles on cache misses. (6%) (b) Assume that the cycle time is 400ps for processors 1 and 2, and 300ps for processor 3. Determine which processor is the fastest and which is the slowest. (4%)

7. **[I/O Communication]** Suppose we want to use a laptop to send 100 files of approximately 50 MB each to another computer over a 5 Mbit/sec wireless connection. The laptop battery currently holds 100,000 joules of energy. The wireless network card alone consumes 5 watts while transmitting, while the rest of the laptop consumes 40 watts. Before each file transfer we need 10 seconds to choose which file to send. How many complete files can we transfer before the laptop's battery runs down to zero? (10%)

8. **[Performance]** Consider a non-pipelined processor whose instruction set contains floating point (FP) instructions. Suppose we have measured the CPI of the FP instructions to be 12, while the average CPI for all other instructions is 5. A proposed enhancement is to reduce the CPI of FP instructions to 6. Another proposed enhancement is to decrease the clock cycle time by 30%. Let f be the fraction of instructions that are FP instructions. For what value of f would the two above enhancements be equivalent? (10%)

9. **[IEEE 754 Representation]** The IEEE 754 floating-point standard specifies 64 bit double precision with a 53-bit significand (including the implied 1) and an 11-bit exponent. IA-32 offers an extended precision option with a 64-bit significand and a 16-bit exponent. (a) Assume extended precision is similar to single and double precision, what is the bias of the exponent? (4%) (b) What is the range of numbers that can be represented by the extended precision option? (6%)

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10. **[Branch Predlction]** We have a program core consisting of four conditional branches. The program core will be executed thousands of times. Below are the outcomes of each branch for one execution of the program core (T for taken, N for not taken.)

- Branch 1: T-T-T
- Branch 2: N-N-N-N
- Branch 3: T-N-T-N-T-N
- Branch 4: T-T-T-N-N

Assume the behavlor of each branch remains the same for each program core execution. For dynamic schemes, assume each branch has its own prediction buffer and each buffer is initialized to the same state before each execution. List the predictions for the following branch prediction schemes and compute the prediction accuracies. (10%)

a. Always taken
b. Always not taken
c. 1-bit predictor, initialized to prediction taken.