國立臺灣師範大學108學年度碩士班招生考試試題

科目：計算機系統　　適用系所：資訊工程學系

注意：1.本試題共 3 頁，請依序在答案卷上作答，並標明題號，不必抄題。2.答案必須寫在指定作答區內，否則依規定扣分。

1. (8 分) Convert the following decimal numbers to unsigned 8-bit binary numbers:
   (a)(4 分) 15
   (b)(4 分)113

2. (10 分) Consider a CPU with clock cycle time of 1 ns. Suppose the CPU executes a program with 500 instructions. The CPU time is 1000 ns for the program.
   (a) (5 分) Find the clock rate of the CPU (in gigahertz, or GHz).
   (b) (5 分) Find the Clock cycles Per Instruction (CPI) for executing the program.

3. (18 分) Consider a RISC processor with separate instruction and data memories. Suppose the following code sequence is executed on the processor.

```
LW    R1,16(R10);     R1 ← MEM[R10+16]
LW    R2,20(R10);     R2 ← MEM[R10+20]
LW    R3,24(R10);     R3 ← MEM[R10+24]
LW    R4,28(R10);     R4 ← MEM[R10+28]
ADD   R5,R1,R2;       R5 ← R1+R2
SUB   R6,R3,R4;       R6 ← R3-R4
ADD   R7,R5,R6;       R7 ← R5+R6
SW    R7,32(R10)      MEM[R10+32] ← R7
```

   (a) (5 分) Determine the number of accesses to the instruction memory,
   (b) (5 分) Determine the number of accesses to the data memory,
   (c) (4 分) Suppose there is only one miss in the instruction memory for the code sequence. Compute the miss rate of the instruction memory.
   (d) (4 分) Suppose there are two misses in the data memory for the code sequence. Compute the miss rate of the data memory.

4. (14 分) Consider a five-stage (IF, ID, EX, MEM and WB) RISC pipeline processor with data hazard detection and data forwarding units. Assume the processor includes separate instruction and data memories so that the structural hazard for memory references can be avoided.

Assume there is no structural hazard. There is also no cache miss. Find the number of clock cycles required by the pipeline for the execution of each of the following sequences.

(a) (7 分)

```
SUB   R8,R6,R4;      R8 ← R6-R4
ADD   R2,R10,R8;     R2 ← R10+R8
ADD   R7,R9,R11      R7 ← R9+R11
```

(b) (7 分)

```
LW    R2,12(R4);     R2 ← MEM[R4+12]
SUB   R8,R10,R2;     R8 ← R10-R2
SW    R8,16(R4);     MEM[R4+16] ← R8
```

5. (10 points) Amdahl's Law is a formula that identifies potential performance gains from adding additional computing cores to an application that has both serial and parallel components. If S is the portion of the application that must be performed serially on a system with N processing cores, what is the maximum speedup?

6. (10 points) Assume that we use demand paging with four frames. Consider the following page reference string.

10 7 12 1 6 2 12 1 10 10 11 2 5 4 10 6 11 3 4 2

How many page faults would occur for the following replacement algorithms?

(a) (5 points) FIFO replacement.

(b) (5 points) LRU replacement.

7. (10 points) Assume that a disk drive has 8000 cylinders, numbered 0 to 7999. The disk drive is currently serving a request at cylinder 150, and the previous request was at cylinder 1850. Consider the following queue of pending requests in FIFO order.

3130 373 6771 7086 3682 3670 2533 6751 2770 835 5852 2924 1813 3030 724

Starting from the current head position, what is the total distance (in cylinders) that the disk arm moves to satisfy all the pending requests for the following disk scheduling algorithms?

(a) (5 points) FCFS scheduling.

(b) (5 points) SSTF scheduling.

8. (10 points) Consider the following processes. Determine the average waiting time of the execution for the following scheduling algorithms.

Process	CPU burst time	Arrival time
P1	8	0
P2	3	3
P3	6	2
P4	5	6
P5	4	7

(a) (5 points) FCFS scheduling.

(b) (5 points) RR scheduling with time quantum = 5 time units.

9. (10 points) Please answer following questions about synchronization.

(a) (5 points) What is a critical section?

(b) (5 points) What are the three requirements of solving a critical-section problem?