國立中正大學
108學年度碩士班招生考試
試 題

[第2節]

系所組別	電磁晶片組 電機工程學系－計算機工程組 晶片系統組
	機械工程學系光機電整合工程
科目名稱	電子學

－作答注意事項－

※作答前請先核對「試題」、「試卷」與「准考證」之系所組別、科目名稱是否相符。

1. 預備鈴響時即可入場，但至考試開始鈴響前，不得翻閱試題，並不得書寫、畫記、作答。
2. 考試開始鈴響時，即可開始作答；考試結束鈴響畢，應即停止作答。
3. 入場後於考試開始40分鐘內不得離場。
4. 全部答題均須在試卷（答案卷）作答區內完成。
5. 試卷作答限用藍色或黑色筆（含鉛筆）書寫。
6. 試題須隨試卷繳還。

國立中正大學 108 學年度碩士班招生考試試題

科目名稱：電子學　　本科目共 2 頁　第 1 頁

系所組別：電機工程學系-電磁晶片組、計算機工程組、晶片系統組
機械工程學系光機電整合工程

1. Assuming the op-amp is ideal, calculate the input impedance R_{in} of the circuit shown in Fig. P1. (10%)

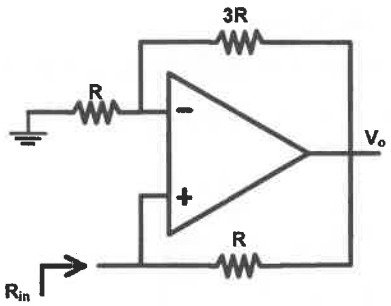

Fig. P1

2. Fig. P2 shows an amplifier with the midband gain A_{vo} = 84dB and the three left-half-plan poles of 50kHz, 500kHz, and 10MHz. The capacitor C_c is for the Miller's compensation.

(a) Draw the Bode diagram (both magnitude and phase) of this amplifier without C_c. (12%)

(b) Find the unity-gain frequency of the open-loop gain without compensation C_c. (10%)

(c) If compensation capacitor C_c is applied as shown in Fig. P2 so that the phase margin is 45° when the transfer ratio of the feedback network β = –18 dB, the second pole after compensation is shifted to 700kHz whereas the pole at 10MHz remains unchanged. Find the required dominant-pole location after compensation. (10%)

(d) Given that the voltage gain of the amplifier is –600 and the node resistance at node k is 200 kΩ,determine the value of C_c to achieve the Miller's compensation with the dominant pole in (c). (8%)

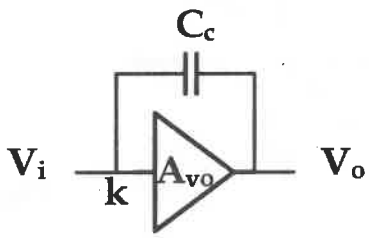

Fig. P2

3. The circuit shown in Fig. P3 is designated with $\mu_n C_{OX}$ = 200 μA/V^2, λ_n = 0, V_{tn} = 0.4V, and $(W/L)_{Q1}$ = 100. Please determine the values of R_1 and R_2. (12%)

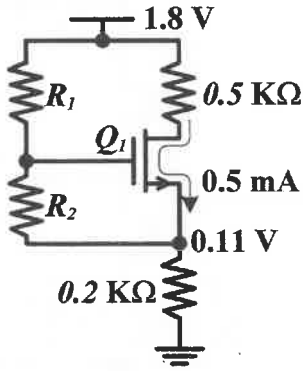

Fig. P3

4. Fig. P4 shows a differential amplifier, which is fabricated with the following parameters: $\mu_n C_{OX} = 2\mu_p C_{OX} = 100\ \mu A/V^2$, $\lambda_n = 0.02V^{-1}$, $\lambda_p = 0.02V^{-1}$, and $V_{tn} = |V_{tp}| = 0.4V$. Assume that all transistors have the same transconductance.

(a) If $(W/L)_{Q1,Q2} = 10$, please determine the differential mode voltage gain (A_d). (14%)

(b) Please modify the circuit of Fig. P4 to improve A_d. (4%)

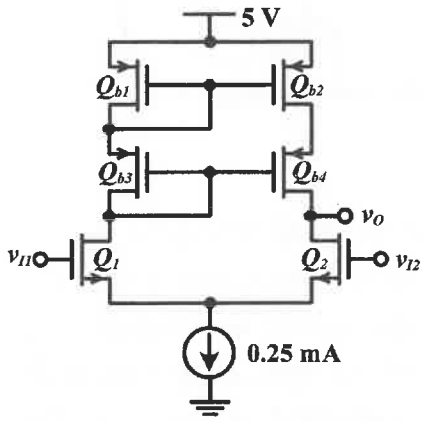

Fig. P4

5. Use diodes, resistors, and voltage sources to design a circuit that has an input/output characteristic shown in Fig. P5. Please consider diodes with the following behaviors:

(a) Ideal diode. (5%)

(b) Diode with $V_{D,on} = 0.7$ V. (5%)

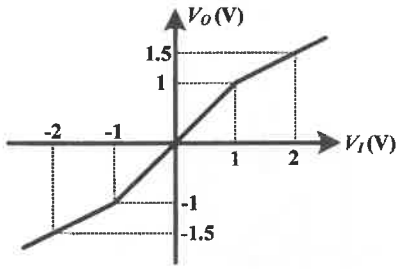

Fig. P5

6. For the circuit shown in Fig. P6, please determine the logic functions (X, Y). (10%)

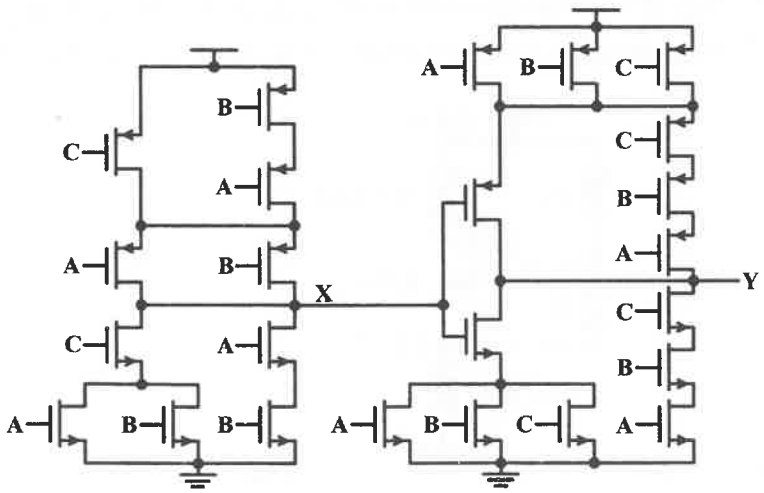

Fig. P6