1. (a) Calculate the bias current (I_D) of M_1 in Fig. 1. Assume $\mu_n C_{ox} = 100\ \mu A/V^2$ and $V_{TH} = 0.4$ V. (10 points)

   (b) If the gate voltage of M_1 increases by 10 mV, what is the change in its drain voltage? (10 points)

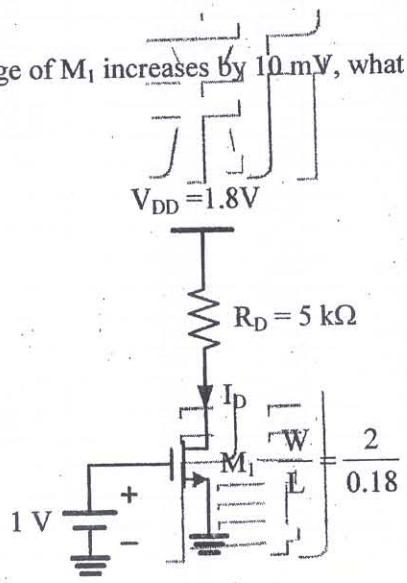

Fig. 1

2. Calculate the CMRR (common-mode rejection ratio) of the circuit shown in Fig. 2. (15 points)

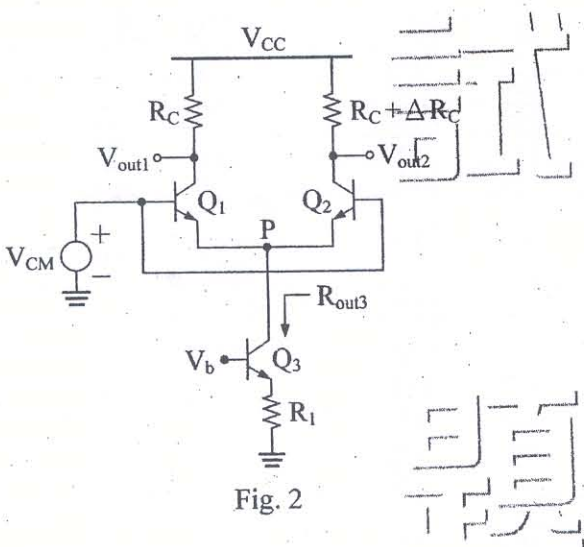

Fig. 2

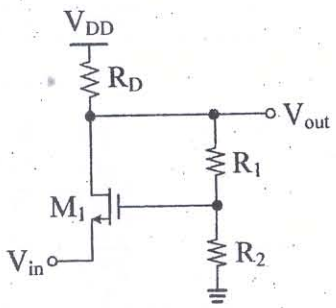

Fig. 3

3. Calculate the voltage gain, input impedance, and output impedance of the amplifier depicted in Fig. 3. Suppose R_1+R_2 is not much less than R_D. (15 points)

4. Fig. 4(a) shows a common-base stage with input capacitor coupling. Prove its frequency response at low frequencies can be represented as that in Fig. 4(b). (15 points)

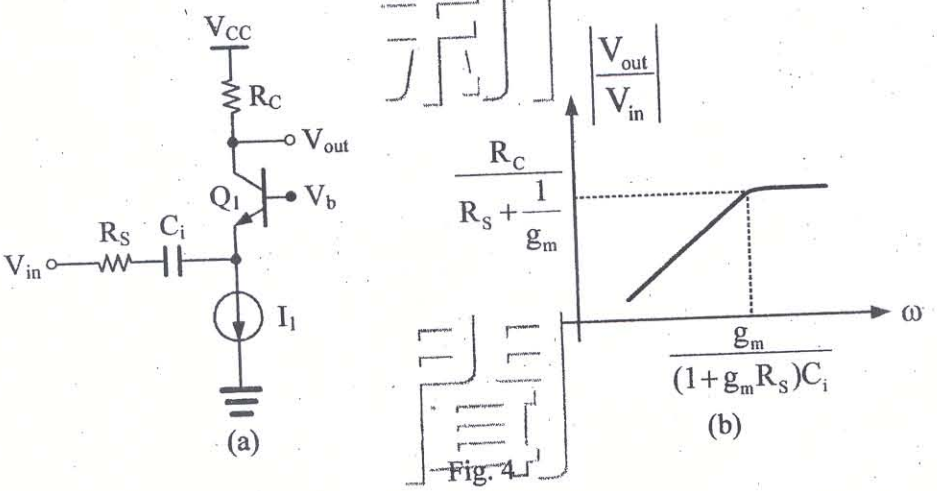

Fig. 4

5. Estimate the poles of the circuit shown in Fig. 5. Assume $\lambda = 0$. (15 points)

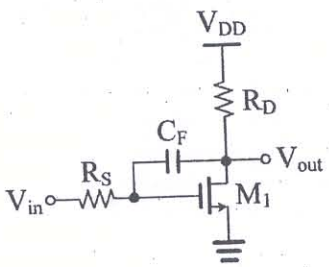

Fig. 5

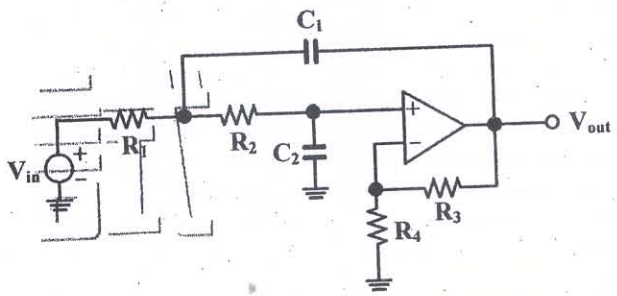

Fig. 6

6. Fig. 6 shows the Sallen and Key filter with in-band gain. Assuming an ideal op amp, determine the transfer function of the circuit. (20 points)