1. (10%) True or False
   a. We can use 8-bit signed 2's complement to express at most 255 different numbers.
   b. In CPU design, the pipelining technique can effectively reduce both clock cycle time and latency.
   c. Both pipelining and instruction-level parallelism (ILP) techniques can increase system throughput.
   d. In memory hierarchy design, the level of the memory hierarchy closest to the CPU is smaller but faster, so L1 cache is smaller and faster than L2 cache.
   e. We consider "Temporal Locality" in cache design because items near those accessed recently are likely to be accessed soon.

2. (10%) The floating-point format to be used in this problem is an 8-bit IEEE 754 normalized format with 1 sign bit, 4 exponent bits, and 3 fraction bits. It is identical to the 32-bit and 64-bit formats in terms of the meaning of fields and special encodings. The exponent field employs an excess-7 coding (Bias = 7). The bit fields in a number are (sign, exponent, fraction). Assume that we use unbiased rounding to the nearest even specified in the IEEE floating point standard.
   a. Encode the binary number, 0.0011011, into the 8-bit IEEE format.
   b. Decode the number in 8-bit IEEE format, 11010101, into the decimal value.

3. (18%) What are structure, data, and control hazards? For each hazard, you need to explain with an example and propose at least two techniques to eliminate the hazard.

4. (12%) Using the code below, list all of the dependence types (RAW, WAR, WAW) between the instructions.

```
I0: A = B + C;
I1: C = A – B;
I2: D = A + C;
I3: A = B × C × D;
I4: C = F / D;
I5: F = A ^ G;
I6: G = F + D;
```

5. (14%) P_1 is a one address accumulator-based machine while P_3 is a three address machine. P_1 and P_3 are conventional computers each with 16 general-purpose registers R0:R15 for data and address storage. All two processors have instructions with the (assembly language) opcodes LOAD, STORE, ADD, SUB, MUL, and DIV to implement the operations +, -,×, and /, respectively. Using as few instructions as you can, write two programs for P_1 and P_3 machines to evaluate the following arithmetic expression: X :=(A/B+C×D)/(A-B).

6. (10%) G_i and P_i are called the generate and propagate , respectively , which are defined by the following logic equations :

   $G_i=x_iy_i$　$P_i=x_i+y_i$　(i=0,1,2.....,n-1) ($C_{in}=0$)

   Give the circuit equation of carry C_0 and C_1 for 3-bit carry lookahead adder.

7. (16%) Booth's algorithm and Modified Booth's Algorithm
   a. Calculate 11101110 X 11001110 by Booth's algorithm.
   b. Find the values of $P_0, P_2, P_4 and P_6$ b y Modified Booth's algorithm.

multiplicand	Y	11101110
multiplier	X	11001110
P_0		
P_2		
P_4		
P_6		
P	$= P_0 + P_2 + P_4 + P_6$	

8. (10%) The performance of a 500MHz microprocessor P is measured by executing 10,000,000 instructions of benchmark code, which is found to take 0.25s. What are the values of CPI and MIPS for this performance experiment?