國立臺北科技大學 100 學年度碩士班招生考試

系所組別：2240 電腦與通訊研究所丁組

第二節　電子學　試題

注意事項：

1. 本試題共四題，配分共 100 分。
2. 請標明大題、子題編號作答，不必抄題。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

一、Consider the design of a CMOS compound AND-OR-INVERT(AOI22) gate:

$F = \overline{(A \bullet B) + (C \bullet D)}$.

1.Sketch a transistor-level schematic. (5%)

2.Assume that the mobility ratio of NMOS and PMOS is 2. Determine the width ratio of NMOS and PMOS to achieve the same falling (0000->1111) and rising (1111->0000) ability. Note that the gate length is the same. (5%)

3.Please use the below layer patterns to layout your gate. (10%)

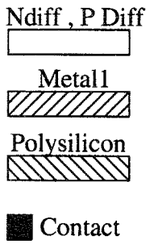

Fig.1 Layer patterns

4.Draw a side view (cross-section) of an typical inverter and annotate the corresponding layer names.(5%)

二、Please answer the questions:

1.Please sketch the transfer characteristic V_o versus V_i for the circuit in Fig.2a. Assume the diodes are ideal. (10%)

2.Please sketch the output waveform of Fig.2b based on the input waveform shown in Fig.2d. Label the most positive and most negative output levels. Assume the diodes are ideal and $RC << T$. (5%)

3.Please sketch the output waveform of Fig.2c based on the input waveform shown in Fig.2d. Label the most positive and most negative output levels. Assume the diodes are ideal and $RC >> T$. (5%)

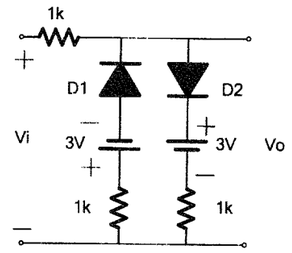

Fig.2a

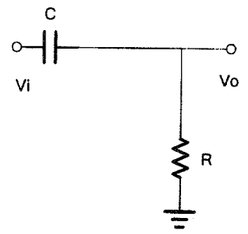

Fig.2b

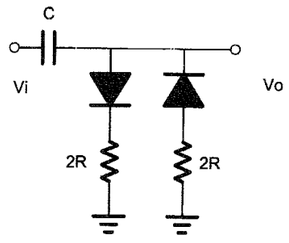

Fig.2c

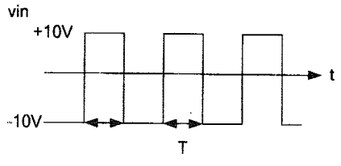

Fig.2d

注意：背面尚有試題

三、Fig.3 shows an output stage of a CMOS op-amp, where V_{DD} = 5V , V_{Bias}=2.5V and C_L = 1nF. Please use these parameters of MOS $|V_{TN}| = |V_{TP}| = 0.7V$,

$\beta_n = \beta_p = 100\mu A/V^2$ and V_A=100V of MOS to calculate the following questions.

$\beta = \mu C_{ox}\frac{W}{L}$.

1.Calculate the input "trip point", which means that the input voltage starts to make V_{out} change sharply. (10%)

2.Calculate the small signal gain $Av = v_o/v_{in}$ when operating at the trip point. (10%)

3.Calculate the negative slew rate when v_o decreased from high to low. (5%)

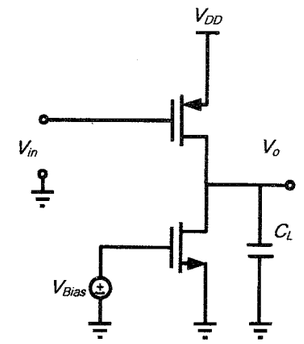

Fig.3

四、According to the active filter shown in Fig.4, please answer the following questions:

1. Find the DC gain of V_o/V_{in}. (5%)
2. Find the transfer function of the voltage gain. (5%)
3. Find the input impedance. (5%)
4. Sketch its magnitude frequency-response characteristics. (5%)
5. Sketch its phase frequency-response characteristics. (5%)
6. Write the transfer function of the input transimpedance (v_o/i_{in}). (5%)

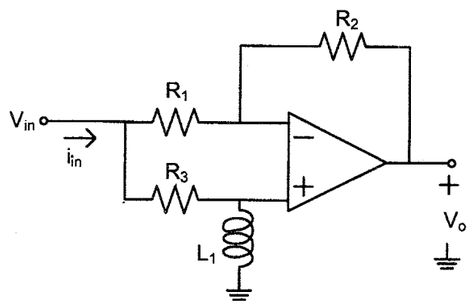

Fig.4