# 國立臺北科技大學 100 學年度碩士班招生考試

## 系所組別：2230 電腦與通訊研究所丙組

## 第二節　電子學　試題



**注意事項**：

1. 本試題共五題，配分共 100 分。
2. 請標明大題、子題編號作答，不必抄題。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

**1.** Assume $M_1$ is in saturation with a transconductance $g_{m1}$ as shown in Fig. 1. Please calculate
**(a)**the input impedance ($Z_{in}$) including gate-to-source capacitance ($C_{gs1}$) and gate resistance ($r_{g1}$). **(10%)**
**(b)**the frequency that $Z_{in}$ is purely inductive or capacitive. **(5%)**

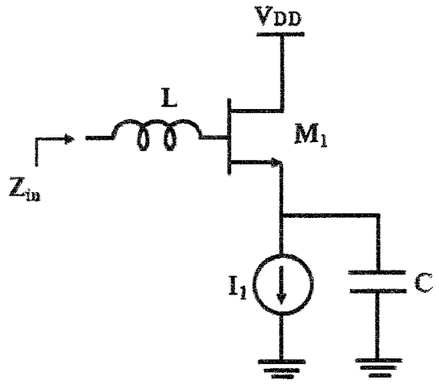


Fig. 1

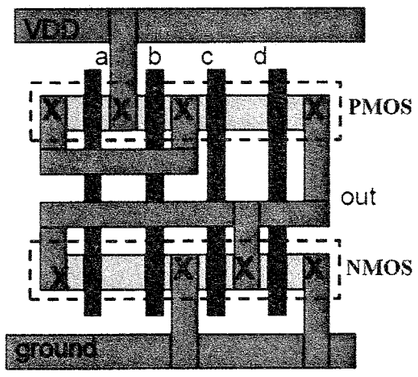


Fig. 2

**2.** Figure 2 shows a layout of a CMOS logic circuit.
**(a)** Sketch the schematic of Fig. 2, where a, b, c, and d are the four inputs, and out is the output **(10%)**
**(b)** What is the logic function in Fig. 2? **(5%)**
**(c)** Why NAND gate is preferably used in CMOS logic circuits as compared with NOR gate for the consideration of package density? **(10%)**

**3.** In the amplifier circuit as shown in Fig. 3, JFET parameters are: $I_{DSS}$=10mA, $V_p$=-1V, $\lambda$=0, $C_{gs}$=$C_{gd}$=0.5pF. Capacitors $C_1$ and $C_2$ are very large. The drain voltage should be biased at $V_D$=5.1V.
**(a)** Find the value of $R_s$. **(6%)**
**(b)** Find the $g_m$ value and mid-band voltage gain $V_o/V_i$. **(6%)**
**(c)** Find the Miller's capacitance $C_M$. **(4%)**
**(d)** Find the upper 3-dB frequency $f_H$. **(4%)**

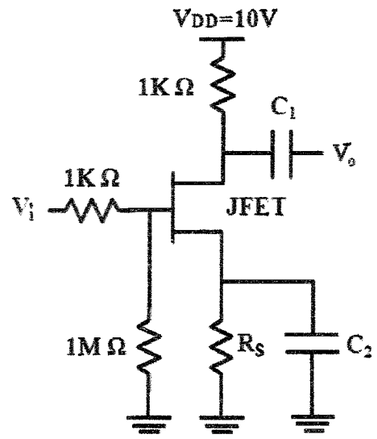


Fig. 3

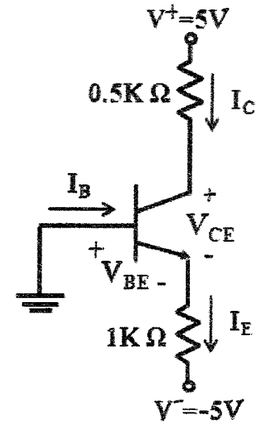


Fig. 4

**4.** For the circuit shown in Fig.4, let $V_{BE(on)}$=0.7V, $\beta$=100, and $V_{CE(sat)}$=0.2V.
**(a)** Determine the $Q$-point of the circuit. **(10%)**
**(b)** Plot the load line and indicate the $Q$-point on the collector current-voltage characteristic plot. Indicate important data and the associated units on the plot. **(10%)**

**5.** In the Fig. 5, the op-amp circuit has three internal critical frequencies as follow: 1.2KHz, 50KHz, and 250KHz. If the midrange open-loop gain is 100dB, is the amplifier configuration stable, marginally stable, or unstable? **(20%)**

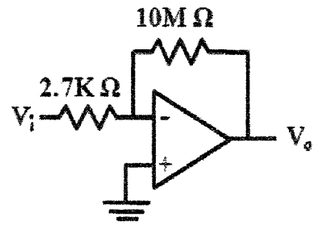


Fig. 5