國立雲林科技大學 系所：資工系
100學年度碩士班暨碩士在職專班招生考試試題 科目：計算機組織

排序題

(1) (5%排序題，順序全對才給分) Please give the correct order of starting up a modern computer system:
   A. BIOS executes Power-On Self-Test (POST) to initialize the hardware devices
   B. Initialize the OS kernel and bring up applications
   C. The boot loader loads the image of an operating system kernel into RAM
   D. BIOS searches for an operating system to boot

問答及計算題

(2) (5%) RAID 1 has the highest check disk overhead among RAID levels 1, 3 and 5. On the other hand, RAID 3 and 5 have the same throughput for large writes. True or false?

(3) (10%) In synchronous processor-memory I/O bus system, the synchronous bus clock cycle time is 50 ns, each bus transmission takes 1 clock cycle, and data bus is 32-bits wide. Find the bandwidth when performing one-word reads from a 200-ns memory.

(4) (10%) Design a three-bit Booth's algorithm.

(5) (5%) Cache thrashing occurs if main memory is accessed in a pattern that leads to multiple main memory locations competing for the same cache lines. This is most problematic for caches that have high associativity. True or false?

(6) (25%) Assume that a 4-way 32KB cache has 128 sets. For a 32-bit architecture, calculate the following: (Please show how you get your answers)
   A. The cache line size (in bytes)? (5%)
   B. How many bits are used for each tag field? (5%)
   C. How many bits are used for each index field? (5%)
   D. How big the entire tag array (in bytes) is needed? (5%))
   E. Now the cache is changed from a 4-way 32KB cache to a fully-associative 32KB cache. For the same 32-bit architecture, how big the entire array (in bytes) is needed? (5%)

   (For (D) and (E), just the tags, you don't not need to account for valid, dirty or LRU bits.)

(7) (10%) Consider a computer has clock rate of 2 GHz. The CPI with a perfect cache is 4. The cache miss penalty is 50 ns. Assume the cache miss rate is 10%. Calculate the following: (Please show how you get your answers)
   A. What is the actual CPI? (5%)
   B. If a second level cache with the 1st level miss penalty 5ns is added, the miss rate to the main memory is reduced to 5%. What is the actual CPI? (5%)

(8) (20%) Consider a computer system with a 500MHz-Clock processor. Its hard disk transfers data in 4-word (16-byte) chunks and can transfer at 4 MB/sec without any transfer lost.
   A. If the system use interrupt-driven I/O, the overhead for each transfer, including the interrupt, is 500 clock cycles. Find the fraction of the processor consumed if the hard disk is only transferring data 5% of the time. (10 %)
   B. If the system uses DMA to transfer data, the initial setup of a DMA transfer takes 1000

clock cycles for the processor, and it assumes the handling of the interrupt at DMA completion requires 500 clock cycles for the processor. The hard disk has a transfer rate 4 MB/sec and use DMA. If the average transfer from the disk is 8KB, what fraction of the processor consumed if the hard disk is actively transferring 100% of the time? Ignore any impact from bus contention between the processor and DMA controller. (10 %)

(9) (10%) Consider a pipeline system.

A. Identify all of the data dependencies in the following code. (5 %)
B. Which dependencies are data hazard that can be resolved via forwarding? (5 %)

```
sub  $2, $1, $3
and  $12, $2, $5
or   $13, $6, $2
add  $14, $2, $2
sw   $15, 100($2)
```