國立高雄應用科技大學
100 學年度碩士班招生考試
資訊工程系

准考證號碼□□□□□□□□□□ （考生必須填寫）

計算機組織與系統

注意：a. 本試卷共 5 題，總分 100 分，試卷共 2 頁。
b. 作答時不必抄題，但須標註題號。
c. 考生作答前請詳閱答案卷之考生注意事項。
d. 請依題號順序作答。
e. 作答過程列入評分。

1. Assume a program consists of 20% load and store instructions, 50% R-type instructions, 20% beq/bne instructions and 10% jump instructions. Furthermore, suppose the accuracy of always-taken branch predictor is 45%, that of always not-taken predictor is 55% and that of 2-bit predictor is 90%. In addition, assume that there are no data hazard, that no delay slots are used, and that branch outcome are generated in the EX stage.

(a) Calculate the values of extra CPI due to mispredicted branches with always-taken, always not-taken, and 2-bit approaches respectively. (10分)

(b) Assume 70% of all executed branch instructions are loop-back branches which are always predicted correctly. Please calculate the accuracy of 2-bit predictor on the remaining 30% of the branch instructions. (10分)

2. Assume that the latency of IF stage in a data path is 400ps; that of ID stage is 250ps; that of EX is 200ps; that of MEM is 600ps and that of WB is 100ps.

(a) Calculate the clock cycle time in a pipelined and single-cycle processor respectively. (10分)

(b) Calculate the total latency of executing only one *lw* instruction in a pipelined and single-cycle processor respectively. (10分)

3. Suppose a processor with the following parameters: base CPI with no memory stall is 1.5; clock rate is 2 GHz; main memory access time is 150 ns; miss rate per instruction at first-level cache is 4%; the direct-mapped and 4-way set associative speed of second-level cache is 15 and 30 cycles respectively; the global miss rates of second-level cache with direct-mapped and 4-way set associative is 3% and 2% respectively. Calculate respectively the CPI for the processor using only a first-level cache, a second-level cache with direct-mapped and a second-level cache with 4-way set associative. (10分)

4. Suppose the processes P1 to P4 are assumed to have arrived in the order P1, P2, P3, P4, all at time 0. In addition, the CPU burst time of P1, P2, P3 and P4 respectively is 7, 1, 4 and 2 milliseconds and the priority of P1, P2, P3 and P4 respectively is 2, 1, 4 and 3.

(a) Draw four Gantt charts that illustrate the execution of these processes using the following scheduling algorithms: FCFS, SJF, nonpreemptive priority (a smaller priority number implies a higher priority), and RR (quantum = 1). (10分)

(b) Calculate the turnaround time of each process for each of the scheduling algorithms in (a). (10分)

(c) Which of the algorithms results in the minimum average waiting time (over all processes)? (5分)

5. Assume two systems S1 and S2 use respectively 2 and 4 frames to support page replacement. Consider the following page reference sequence:

   1, 2, 3, 2, 1, 2, 4, 5, 2, 1, 3, 2, 4, 3, 2, 1, 2, 3, 4.

   Calculate the number of the occurrence of page faults for FIFO, LRU and Optimal replacement algorithms respectively. (25分)