國立彰化師範大學 100 學年度碩士班招生考試試題

系所：電子工程學系　　組別：乙組　　科目：計算機組織

☆☆請在答案紙上作答☆☆　　

1. Simplify the logic circuit in Fig. 1:
   A. Derive the Boolean function or Truth table (5%)
   B. Show the simplified circuit (5%)

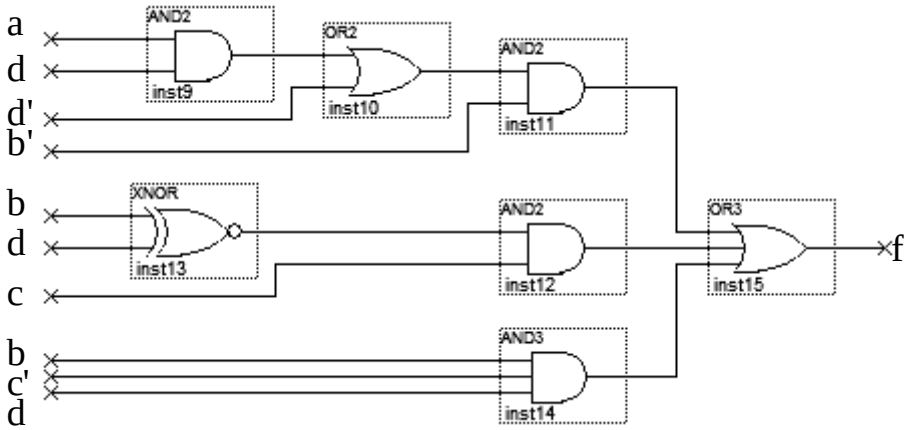

Fig. 1 A combinational logic circuit

2. Derive the state table and state diagram of Fig. 2 (10%)

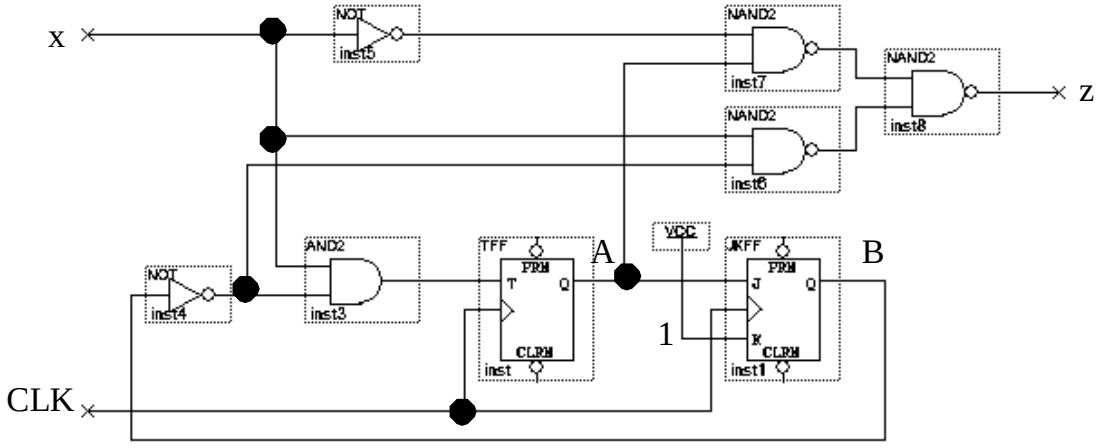

Fig. 2 A sequential logic circuit

3. For each of the following functions

a	*b*	*c*	*f*	*g*
0	0	0	0	1
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	0

A. Show the SOP (Sum of Product) canonical form of functions. (5%)
B. Show the simplified Boolean functions. (5%)

4. Reduce the following sequence system to have the minimum number of states (10%)

q_n	q_{n+1}		z	
	$x=0$	$x=1$	$x=0$	$x=1$
A	B	D	0	0
B	E	G	1	0
C	G	F	0	0
D	A	C	1	1
E	B	D	0	0
F	G	D	0	0
G	A	B	1	0

5. Design synchronous counter that go through the following sequence:
1→3→4→7→6→1→3→4→7→6→1→… (10%)

6. Suppose you are trying to improve the performance of processor X, which spends 25% of its CPU time executing floating point (FP) operations and 30% of its CPU time executing the load/store operations. The first improvement method is to make the FP operations run 10 times faster, and the second improvement method is to make the load/store operations run 7 times faster. (10%)
(a)Which method (the first or the second) can get higher speed-up?
(b)Suppose the floating point operations can be improved by a factor of infinity (∞), what is the speed-up?

7. Translate the following C code segment into MIPS assembly code (10%)

```
while ( j < 10)
    {if (A[j]>=B[j])
        {sum = sum + A[j];}
     else
        {sum = sum + B[j];}
     j=j+1; }
```

Assume variable *j* is assigned to *R1* and variable *sum* is assigned to *R2*; the start address of integer array *A* is already stored in *R3*; the start address of integer array *B* is already stored in *R4*.

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8. Figure 3 shows the block diagram of processor MIPS R2000 (Figure 3 is from the book *Computer Organization and Design* by Patterson and Hennessy). If the processor is executing the instruction LW R11, 56(R7), what are the values for the following signals? (a) Instruction[25-21]; (b) Instruction[20-16]; (c) Instruction[15-0]; (d) ALUSrc; (e) MemtoReg. (10%)

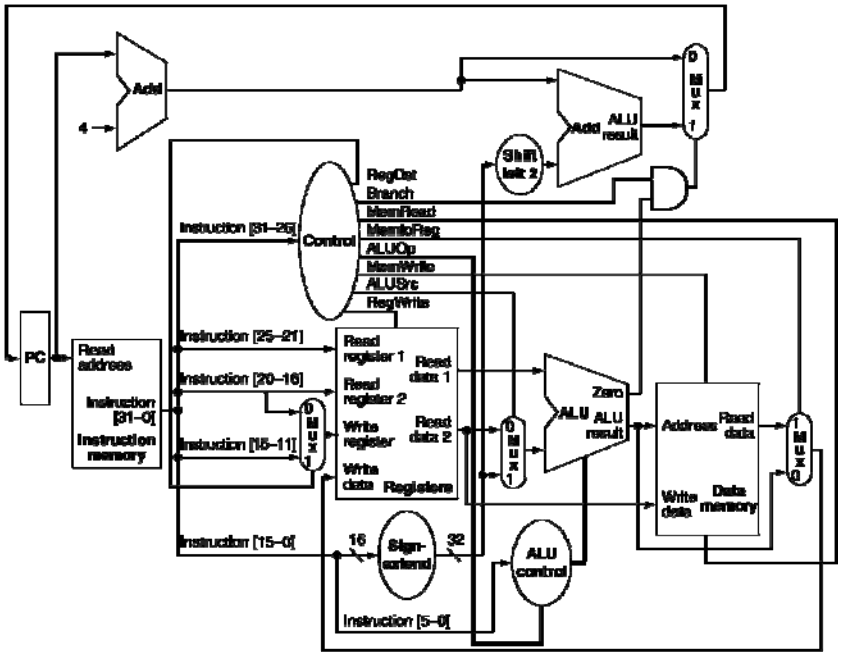

Figure 3: block diagram of processor MIPS R2000

9. Plot the block diagram for *4-way set-associative cache* and explain how the address, which is composed of *tag*, *index*, and *offset*, sent from the processor is used to access the cache. (10 %)

10. Explain how virtual memory is implemented in a computer system. You must explain (a) page table; (b) address translation; (3) the advantages of virtual memory. (10%)