國 立 宜 蘭 大 學

107學年度研究所碩士班考試入學

電子學 試題

(範圍相當於 Sedra/Smith 微電子學前七章)

(電子工程學系碩士班)

准考證號碼:

《作答注意事項》

- 1.請先檢查准考證號碼、座位號碼及答案卷號碼是否相符。
- 2.考試時間:100分鐘。
- 3.本試卷共有 6 題,第 1 題為 10 個單選題,每題 4 分,小計 40 分,第 2~6 題為非選擇題,小計 60 分,合計 100 分。
- 4.請將答案寫在答案卷上。
- 5.考試中禁止使用手機或其他通信設備。
- 6.考試後,請將試題卷及答案卷一併繳交。
- 7.本試卷採雙面影印,請勿漏答。
- 8.本考科可使用非程式型(不具備儲存程式功能)之電子計算機。

107學年度研究所碩士班考試入學 電子工程學系碩士班

電子學(範圍相當於 Sedra/Smith 微電子學前七章)考科 第1頁,共2頁

- Choose the correct answer for the following questions. (40%) 1.
 - (1) Consider the amplifier shown in Fig. 1.(1) with ideal op amps and $R_1 = 1 \text{ k}\Omega$, $R_2 = 3 \text{ k}\Omega$, $R_L = 1 \text{ k}\Omega$. If $v_I = 1 \text{ V}$. Then current $i_2 = ?$ (A) 0.5 mA (B) 1 mA (C) 1.5 mA (D) 2 mA
 - (2) Continuing the above problem, current $i_L = ?$ (A) 1 mA (B) 2 mA (C) 3 mA (D) 4 mA
 - (3) If the circuit shown in Fig. 1.(3) is an ideal diode circuit, which is the correct transfer characteristic? In the figures, m is the slope.

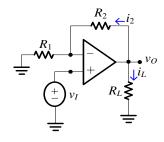


Fig. 1.(1)

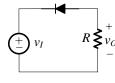
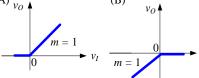
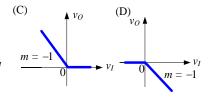


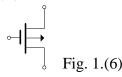
Fig. 1.(3)





- (4) For BJT, the h_{FE} is defined as (A) $\frac{I_C}{I_R}$ (B) $\frac{\Delta i_C}{\Delta i_R}$ (C) $\frac{I_C}{I_E}$ (D) $\frac{\Delta i_C}{\Delta i_E}$
- (5) The BJT's finite output resistance in active region, r_o , results from (A) Early effect (B) Avalanche effect (C) Temperature effect (D) Zener Effect.
- (6) The symbol shown in Fig. 1.(6) stands for

 - (A) enhancement-type NMOS (B) enhancement-type PMOS
 - (C) depletion-type NMOS
- (D) depletion-type PMOS.

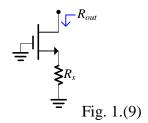


- (7) An enhancement-type NMOS FET, with $V_t = 1 \text{ V}$ and $k_n' = 25 \mu\text{A/V}^2$, has its source terminal voltage = 0.5 V and a 2.5 V dc applied to the gate. What region does the device operate for $V_D = 1 \text{ V}$? (A) Saturation (B) Cutoff (C) Triode (D) Active region.
- (8) If a depletion-type NMOS FET is in saturation region, and its current is

$$i_D = \frac{1}{2}k_n(v_{GS} - V_t)^2 \cdot (1 + \lambda v_{DS})$$
. Which is correct?

(A) $V_t > 0$

- (B) k_n is in proportion to L/W
- (C) λ is related to the Miller effect (D) $v_{GS} > V_t$
- (9) In Fig. 1.(9), if $R_s = r_o = 10 \text{ k}\Omega$, $g_m = 2 \text{ mA/V}$, then $R_{out} = ?$ (A) $2 k\Omega$ (B) $20 k\Omega$ (C) $200 k\Omega$ (D) $400 k\Omega$



- (10) Which is correct about CB (Common Base) amplifier?
 - (A) large input resistance
- (B) bad high frequency response
- (C) high voltage gain
- (D) used as voltage buffer

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電子學(範圍相當於 Sedra/Smith 微電子學前七章)考科

第2頁,共2頁

- 2. If the circuit shown in Fig.2 has $R_a = 2 \text{ k}\Omega$, $R_b = 50 \text{ k}\Omega$, and C = 2 nF.
 - (a) What is the circuit?
 - (b) Find its transfer function $V_o(s)/V_i(s)$.

(10%)

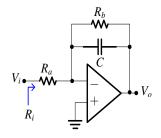
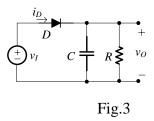


Fig.2

- 3. Consider a peak rectifier, shown in Fig.3, fed by a 60 Hz sinusoid v_I having a rms value $V_{\rm rms} = 24$ V. Let the load resistance $R = 10 \text{ k}\Omega$.
 - (a) Find the capacitance *C* that will result in a peak-to-peak ripple of 2 V.
 - (b) Find the peak value of the diode current $i_{D,\max}$.

(10%)



4. For the circuit shown in Fig.4 has that $V_{CC} = +9$ V, $R_B = 100$ k Ω . If the β of transistor is specified the range of 50 to 200, (a) find the maximum value of R_C so that the circuit is in the active mode.(b) Continuing the above problem, what is the range of collector voltage V_C ?

(10%)

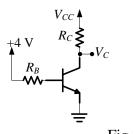
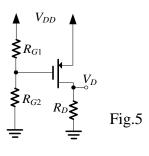


Fig.4

- 5. For the circuit shown in Fig.5, let $V_{DD} = 5$ V. The FET operates in saturation with $I_D = 0.25$ mA, and has $V_{tp} = -1$ V, $\mu_p C_{ox}(W/L) = 1$ mA/V². Find
 - (a) $|V_{GS}|$.
 - (b) What is the largest value that R_D can have while maintaining saturation region operation?

(10%)



- 6. (a) Design the CE amplifier, shown in Fig.6, to obtain DC current $I_E = 0.5$ mA for $V_{CC} = +10$ V, $V_C = 6$ V, $V_B = 3$ V, $\beta = 100$, and current through R_{B2} of 50 μ A.
 - (b) What is the function of C_1 and C_2 ?
 - (c) Find input resistance R_{in} .
 - (d) If $R_L = 20 \text{ k}\Omega$, find $A_v = v_o/v_i$.

(20%)

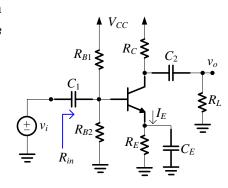


Fig.6