國立高雄師範大學 100 學年度碩士班招生考試試題

（請用藍、黑色筆作答，以其他顏色或鉛筆作答者不予計分）

系所別：電子工程學系

科　目：電子學（第 1 頁，共 2 頁）

1.（a）Explain the Early Effect in BJT.（5%）
（b）How to decrease the effect?（5%）

2. In Si material, the electron and hole mobility are μ_n and μ_p, respectively. Which value is the larger? Please explain it.（5%）

3. In Fig.1, V_{CC} = 10 V, R_B = 930 KΩ, R_C = 10 KΩ, β = 150, find emitter current I_E, input impedance Z_i, current gain A_i, and voltage gain A_V.（15%）

4. The NMOS and PMOS transistors in Fig.2 are matches with $k_n'(W_n/L_n) = k_p'(W_p/L_p) = 1mA/V^2$ and $V_{tn} = -V_{pn} = 1V$. Assuming $\lambda = 0$ for the both devices, find the drain currents i_{DN}, i_{DP} and the voltage v_0 for v_I = 0, +2.5V, and –2.5V.（20%）

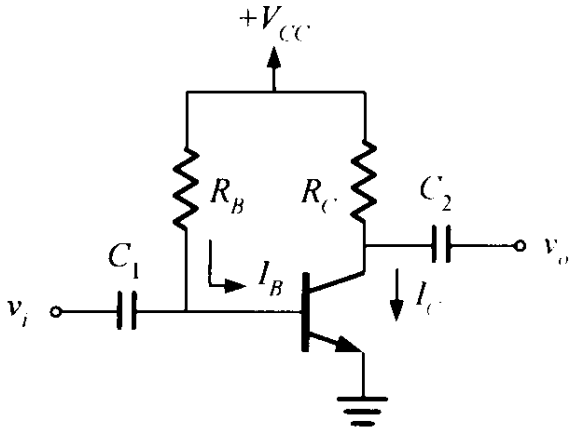

Fig.1

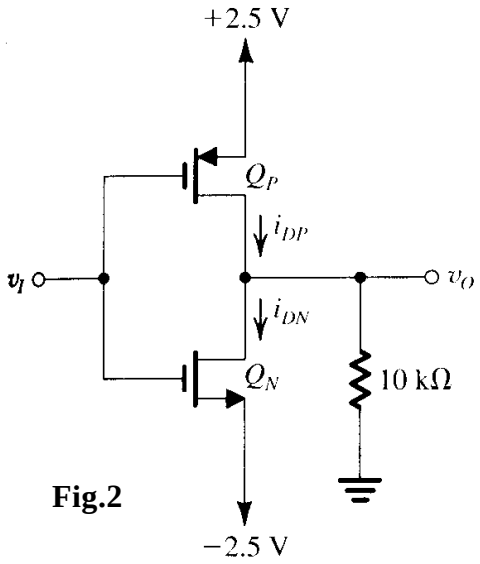

Fig.2

5. For the MOS differential pair with a common-mode voltage v_{CM} applied, as shown in Fig.3, let V_{DD}=V_{SS}=2 V, $k'_n(W/L)$=4 mA/V^2, V_t=0.7 V, I=0.6 mA, and R_D=2.5 kΩ, and neglect channel-length modulation.
(a) Find V_{GS} for each transistor.（4%）
(b) For v_{CM} =+1 V, find v_s, i_{D1}, and v_{D1}.（6%）
(c) What is the highest value of v_{CM} for which Q1 and Q2 remain in saturation?（4%）
(d) If current source I requires a minimum voltage of 0.4 V to operate properly, what is the lowest value allowed for v_s and hence for v_{CM}?（4%）

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6. Consider the circuit of Fig.4 for the case: I=200 μA and V_{OV}=0.25 V, R_{sig}=200 kΩ, R_D=50 kΩ, C_{gs}=C_{gd}=1 pF.
   (a) Find the dc gain.（4%）
   (b) Find the high-frequency poles.（6%）
   (c) Find an estimate of f_H.（4%）

7. For the circuit of Fig.5, the op amp has open-loop gain μ=10^4 V/V, R_{id}=100 kΩ, and r_o= 1 kΩ. Use the feedback method to find:
   (a) The voltage gain V_O/V_S.（5%）
   (b) The input resistance R_{in}.（4%）
   (c) The output resistance R_{out}.（4%）

8. Sketch a pseudo-NMOS realization for the function $Y = \overline{A(B+CD)}$.（5%）

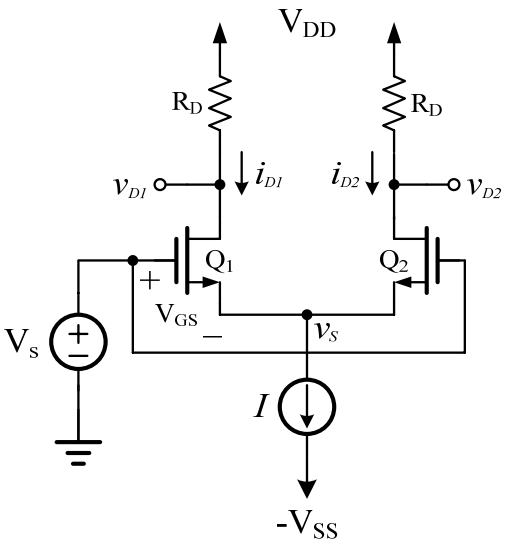

Fig.3

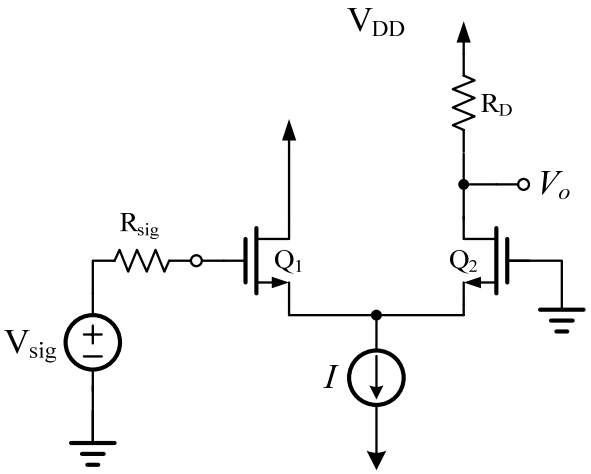

Fig.4

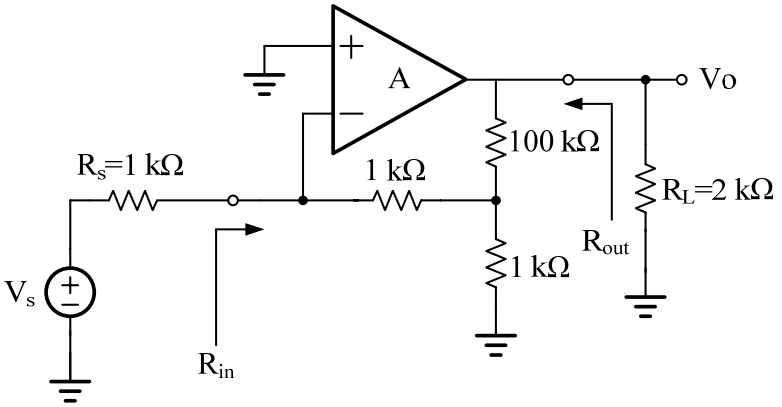

Fig.5