國立臺灣師範大學 100 學年度碩士班招生考試試題

科目：電子學　　適用系所：應用電子科技學系

注意：1.本試題共 4 頁，請依序在答案卷上作答，並標明題號，不必抄題。2.答案必須寫在指定作答區內，否則不予計分。

1. (20 points) Assume that $v_i(t) = 10\sin 2\pi t$, V. Sketch and label the voltage transfer characteristics of the circuits shown in Fig. 1.

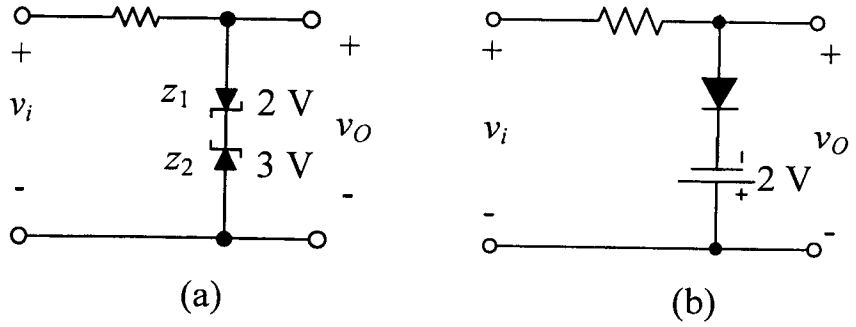


Fig. 1

2. (20 points) In the circuit of Fig. 2, v_{sig} is a small sine-wave signal with zero average. The transistor β is 100 and V_{BE} is 0.7 V.

(a)Find R_E and R_C to establish a dc emitter current $I_E = 0.5$ mA and a dc collector voltage $V_C = +5$V.

(b)For the transistor r_o = 20 kΩ, draw the small-signal equivalent circuit of the amplifier and find the voltage gain v_o/v_{sig}.

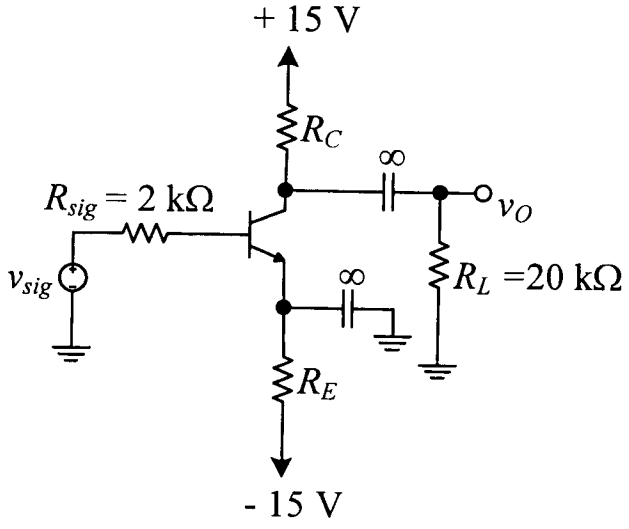


Fig. 2

3. (10 points) Figure 3 shows a Miller integrator. If the integrator capacitor is shunted by a resistor R_F, how will the transfer function be modified? How will the frequency of the integrator pole be changed?

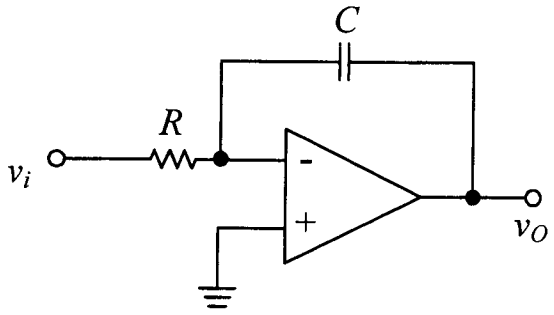


Fig. 3

4. (20 points) Consider the two-stage CMOS opamp in Fig. 4 with the following device geometries (in μm).

Transistor	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
W/L	20/0.2	20/0.2	6.25/1	6.25/1	100/2	25/1	100/1	100/2

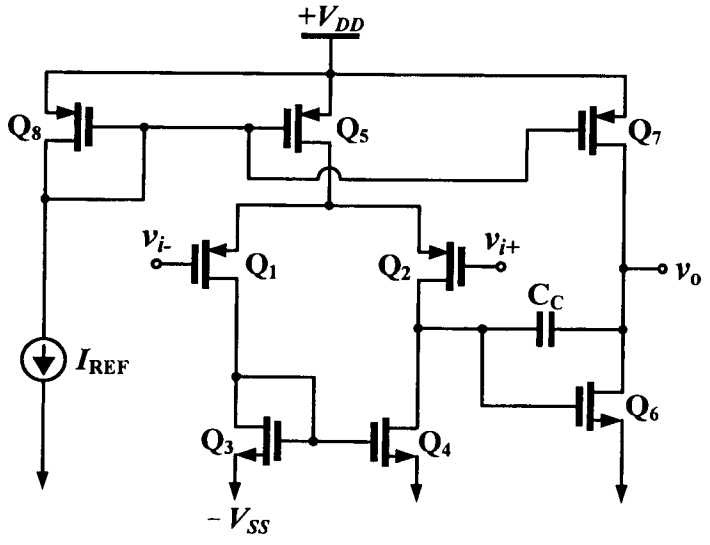


Fig. 4

Let $I_{REF} = 90$ μA, $V_{tn} = 0.45$ V, $V_{tp} = -0.45$ V, $\mu_n C_{ox} = 400$ μA/V^2, $\mu_p C_{ox} = 100$ μA/V^2, $V_{DD} = 1.8$ V, $V_{SS} = 0$ V, and $|V_A| = 10$ V.

(a) For devices Q_2, and Q_6, evaluate I_D, $|V_{GS}|$, g_m, and r_o. Neglect the effect of V_A

on all bias currents.

(b) Find the overall dc open-loop voltage gain $A = v_o/(v_{i+} - v_{i-})$.

(c) Also find the input common-mode range, and the output voltage range.

(d) What are the slew rate and unity-gain frequency of this opamp if C_C = 1.6 pF?

5. (20 points) A voltage-to-current converter employing series-series feedback via resistor R_F. The p-channel MOSFETs, Q_3 and Q_4, have the same dimension (W/L), and the n-channel MOSFETs have the dimension (W/L) shown in Fig. 5. Now, all MOSFETs are operated in saturation region and $\mu_n C_{ox}$ = 20 μA/V^2, $|V_t|$ = 1 V, $|V_A|$ = 100 V for all MOSFETs.

(a) What is the value of I_o/V_s obtained for large loop gain?

(b) Use feedback analysis to find a more exact value for I_o/V_s.

(c) If the output voltage is taken at the source of Q_5, what closed-loop voltage gain is realized?

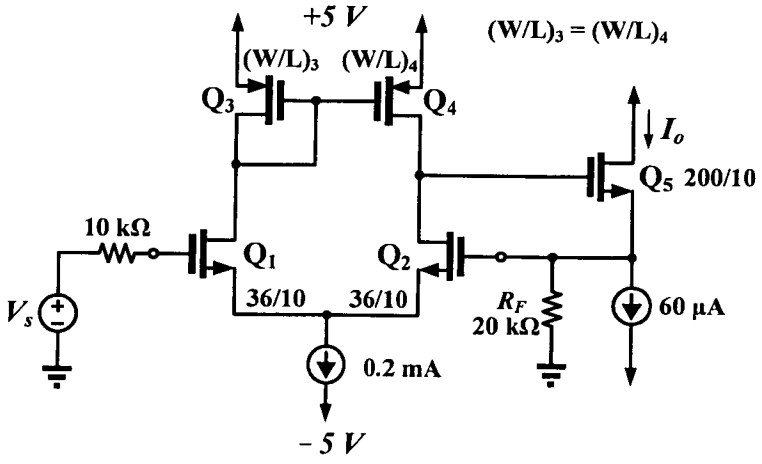
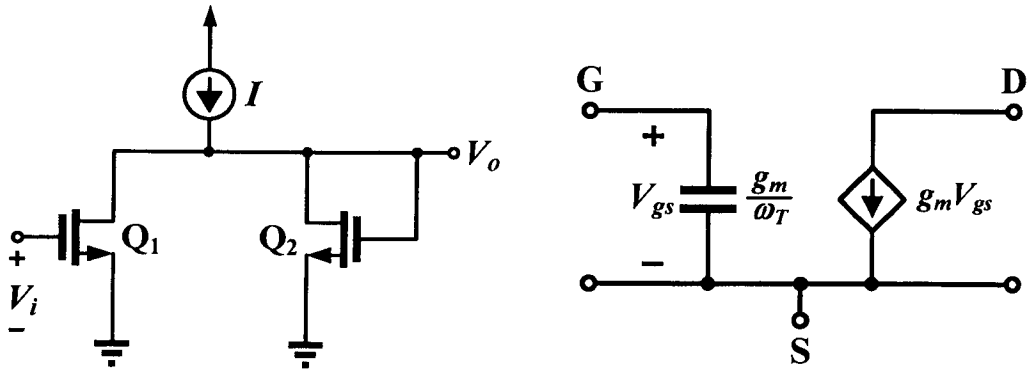


Fig. 5

6. (10 points) Consider a wideband low-gain amplifier stage, as shown in Fig. 6(a). Transistors Q_1 and Q_2 have the same threshold voltage V_t, the same channel length L but different widths W_1 and W_2. They are biased at the same V_{GS} and have the

same unity-gain bandwidth ω_T. Use the MOSFET equivalent circuit of Fig. 6(b) to model this amplifier stage assuming that its output is connecting to the input of an identical stage. Prove that the voltage gain V_o/V_i is

$$\frac{V_o}{V_i} = \frac{-g_{m1}/g_{m2}}{1+\dfrac{s}{\omega_T \Big/ (1+\dfrac{g_{m1}}{g_{m2}})}}$$



(a) (b)

Fig. 6.