1. In each of the following statements, determine whether the statement is **True** or **False**. **Describe your reasons to support your choices**.

(a) By using negative feedback, voltage amplifiers are less sensitive to variations in the amplifier's open-loop gain. (5%)

(b) In amplifiers employing negative feedback, frequency compensation is a technique used to extend the closed-loop bandwidth. (5%)

(c) For a single-pole operational amplifier, the gain bandwidth product is a constant. (5%)

2. Consider the amplifier shown in Fig. P2,

(a) Draw the large signal behavior of V_{out} versus V_{in} (8%)

(b) Draw the small signal equivalent circuit (8%)

(c) Derive the voltage gain V_{out}/V_{in} (2%)

(d) How to maximize the voltage gain? (2%)

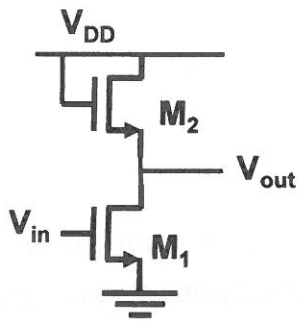

Fig. P2

3. For the amplifier described by the open-loop transfer function $A(s)$ as below, where $p1 = 10^5$ Hz, $p2 = 10^6$ Hz, $p3 = 10^7$ Hz, this amplifier is used with a frequency-independent feedback network β.

$$A(s) = 10^5 / (1+\frac{s}{p1})\ (1+\frac{s}{p2})\ (1+\frac{s}{p3})$$

(a) Draw the Bode plots (both magnitude and phase plots) of $A(s)$ (8%)

(b) What is the closed-loop voltage gain that can be obtained for phase margin of 72° ? (7%)

4. Find the close-loop gain of the feedback current amplifier shown in Fig. P4 in case the transconductance is 4 mA/V for Q_1 and Q_2 while ignoring channel length modulation. (15%)

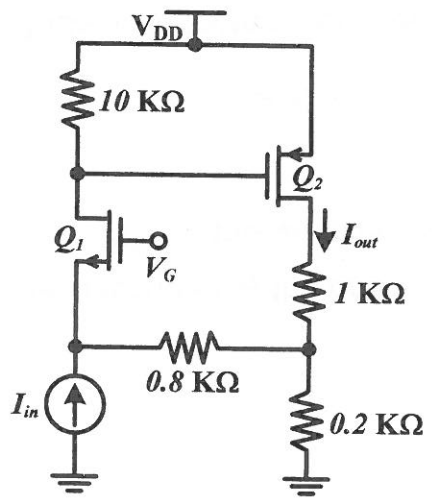

Fig. P4

5. A piece of n-type silicon with uniform doping concentration $N_D = 10^{17}/cm^3$ is fabricated. If we have a voltage of 1 V across it as shown in Fig. P5, using $n_i = 1.5 \times 10^{10}/cm^3$, $\mu_p = 480$ $cm^2/V{\cdot}s$, and $\mu_n = 1350$ $cm^2/V{\cdot}s$ to answer the following questions:

(a) What kind of current is produced? (3%)

(b) Compute the total current density. (6%)

(c) Compute the resistivity of this n-type silicon. (6%)

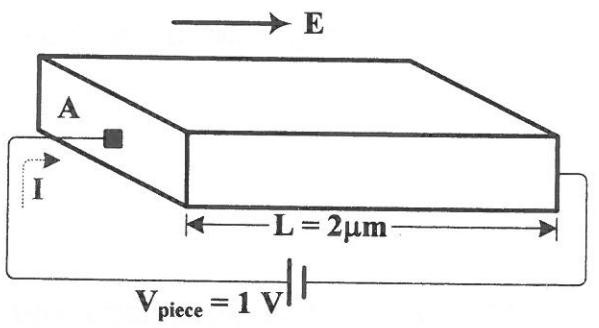

Fig. P5

6. For the circuits shown in Fig. P6, assume $V_{DD} = 1.8$ V, $\mu_n C_{ox} = 100$ $\mu A/V^2$, $\mu_p C_{ox} = 50$ $\mu A/V^2$, $V_{tn} = |V_{tp}| = 0.4$ V, $\lambda = 0$ V^{-1}, $(W/L)_{Q1} = 50$, $(W/L)_{Q2} = 100$, and $R_D = 1$ KΩ.

(a) Please sketch the voltage transfer characteristic (VTC) for each circuit in Fig. P6. (2%)

(b) Assume that input (V_i) has zero rise/fall time and the output time constant is 50 ps for Fig. P6(a), compute the load capacitance and the corresponding low-to-high propagation delay. (6%)

(c) Assume $V_i = 0$ V for the circuit shown in Fig. P6(b), compute the output voltage level. (6%)

(d) For the situation in (c), compute the static power consumption. (6%)

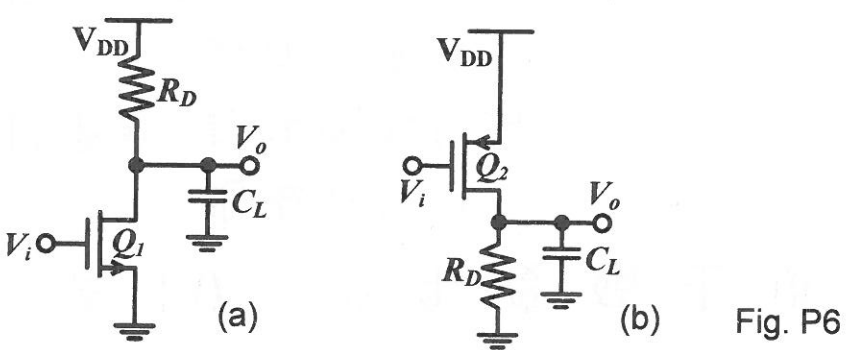

Fig. P6