1. (20%) Please tell the difference of operations in CPU as follows:

   (a). Cycle time & response time, (b). Load instruction & store instruction for data memory, (c). Instruction memory & register file, (d). Single- & Multi-cycle CPU

2. (10%) Please compute the following arithmetic in binary format and then answer in decimal number at the end:

   (a) 56+35 (b) -56+35, (c) 41.6875 + 0.75 (d) 1.45×1.12

3. (20%) Assume a pipelined CPU is designed with basic five stages datapath and the latencies:

Instruction Fetch (IF)	Instruction Decode (ID)	Execution (EX)	Memory Access (MEM)	Write-back (WB)
200ps	280ps	220ps	300ps	250ps

   3.1 (10%) What are the clock cycle time in a non-pipelined and pipelined CPU?

   3.2 (10%) Assume that instructions executed by the processor are broken down for add (25%), sub (20%), j (5%), beq (15%), lw (25) and, sw (10%). Assume there are no stalls or hazards, what is the utilization of the write-register port of the "Register" unit?

4. (10%) Explain the difference between spatial locality and temporal locality during memory access. Please also give example pseudo codes respond to spatial locality and temporal locality, respectively.

5. (10%) Explain why multilevel cache is better than single-level cache. Please analyze the system performance with multilevel cache and single-level cache, respectively, by giving a reasonable example.

6. (10%) The following MIPS code is executed on a processor with a 5-stage pipeline, full forwarding, and a predict-taken branch predictor.

```
        lw    r2, 0(r1)
label1: beq   r2, r0, label2 # not taken once, then taken
        lw    r3, 0(r2)
        beq   r3, r0, label1 # taken
        add   r1, r3, r1
label2: sw    r1, 0(r2)
```

   Draw the pipeline execution diagram for this code by assuming that branches execute in the EX stage.

7. (10%) Schedule the following codes for a dual-issue MIPS processor with loop unrolling, where the loop index is a multiple of three. The processor can fetch one ALU/branch instruction and one load/store instruction at each clock cycle. Please calculate average instructions per cycle based on your result.

```
Loop:   lw    $t0, 0($s1)      # $t0=array element
        addu  $t0, $t0, $s2    # add scalar in $s2
        sw    $t0, 0($s1)      # store result
        addi  $s1, $s1,–4      # decrement pointer
        bne   $s1, $zero, Loop # branch $s1!=0
```

ALU/branch	Load/store	Cycle

8. (10%) Given the following sequence of instructions, if there's full forwarding in the MIPS pipelined processor, specify the signal values of "ForwardA" and "ForwardB" at each clock cycle (CC) from CC1 to CC7. Assume that the first instruction is fetched at CC1.

or r1, r2, r3
or r2, r1, r4
or r1, r1, r2