國立中山大學 107 學年度碩士暨碩士專班招生考試試題

科目名稱：計算機結構【電機系碩士班己組】　　題號：431007

※本科目依簡章規定「可以」使用計算機（廠牌、功能不拘）（問答申論題）　　

1. [15%] Complete the calculations of the following two numbers, X=134.0625, Y=-18

(a) [5%] Represent X and Y using IEEE 754 single precision format, respectively

(b) [5%] Add X and Y, and represent the result using IEEE 754 single precision format

(c) [5%] Multiply X and Y, and represent the result using IEEE 754 single precision format

2. [20%] Translate the following C code to the **minimum** MIPS assembly instructions

```
int A[30], B[30];
for (i=1; i < 30; i++) {
A[i] = A[i] - B[A[i-1]]+i;
}
```

At the beginning of this code segment, the only values in registers are the base address of arrays A and B in registers $a1 and $a2. Assume that the values of i is stored in the register $s0

3. [20%] Figure 1 shows a complete datapath with control for MIPS CPU.

(a) [5%] Explain **in detail** how the architecture shown in Figure 1 is used to execute an I-type instruction (e.g., addi $s3, $s3, 1) **step-by-step**.

(b) [5%] Explain **in detail** how the architecture shown in Figure 1 is used to execute a jump instruction (e.g., j L1) **step-by-step**.

(c) [5%] Describe **in detail** how this architecture is used to execute a load instruction (e.g., lw $t0, 32($s3)) **step-by-step**.

(d) [5%] Explain **in detail** how the architecture shown in Figure 1 is used to execute a branch instruction (e.g., beq $t0, $s5, Exit) **step-by-step**.

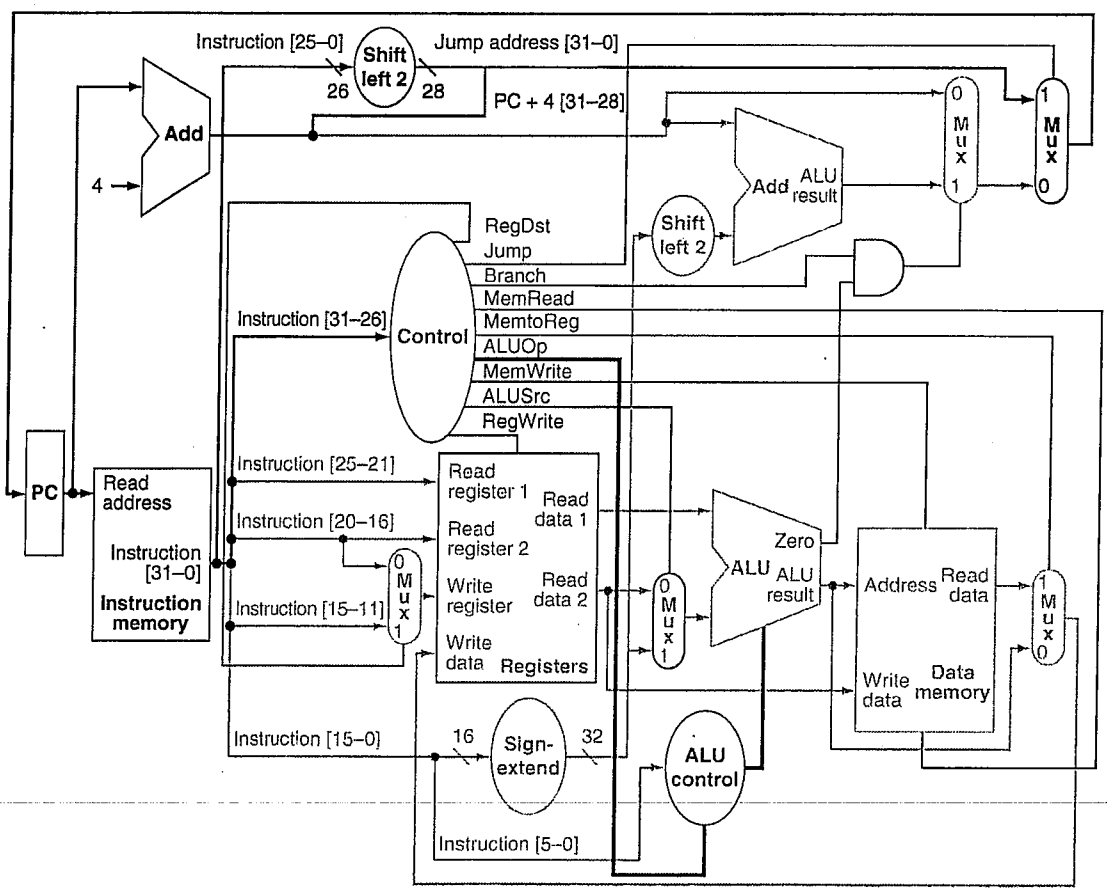

Figure 1: Architecture for Problem 3

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4. [20%] Design of a pipelined-CPU

(a) [5%] Explain the functions of the five pipeline stages of the pipelined MIPS CPU, respectively.

(b) [6%] Use examples to explain the three types of hazards of the pipelined MIPS CPU, respectively.

(c) [9%] Explain **in detail** how we can solve the three types of hazards of the pipelined MIPS CPU based on the architecture shown in Figure 2, respectively.

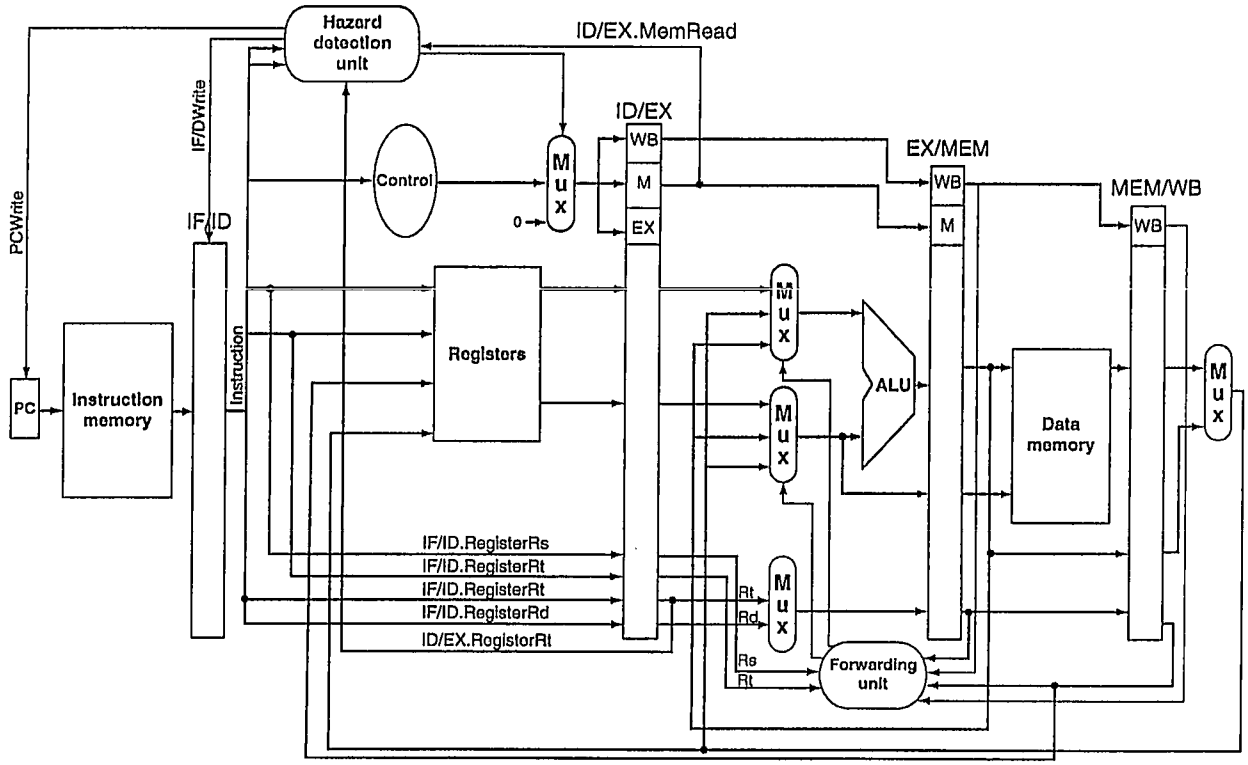

Figure 2: Architecture for Problem 4

5. [25%] Cache memory

(a) [4%] Explain what two localities of memory data are and give examples, respectively.

(b) [2%] Explain how a hierarchical memory system takes advantage of localities.

(c) [4%] What are the advantages and disadvantages of SRAMs and DRAMs, respectively? How are they used in a hierarchical memory system, respectively?

(d) [15%] For a cache with 4 blocks, complete the cache access results for a direct mapped cache, a 2-way set associative cache and a fully associative cache, respectively, shown in the three tables shown below. Please draw these three tables in your answer papers and fill in your answers. Note that in this problem the least recently used block replacement policy is assumed.
請特別注意！請將第三頁表一、表二、 表三的內容繪製在答案卷中並填入答案才允予計分。填寫在題目卷上將不予計分。

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Table 1: Direct mapped cache

Block address	Cache index	Hit/miss	Cache content after access (Mem[x] where x is the block address)			
			0	1	2	3
4						
2						
4						
1						
3						
5						
3						
1						

Table 2: 2-way set associative cache

Block address	Cache index	Hit/miss	Cache content after access (Mem[x] where x is the block address)			
			Set 0		Set 1	
4						
2						
4						
1						
3						
5						
3						
1						

Table 3: fully associative cache

Block address	Hit/miss	Cache content after access (Mem[x] where x is the block address)			
4					
2					
4					
1					
3					
5					
3					
1					