編號： 189

國立成功大學 107 學年度碩士班招生考試試題

系　　所：電腦與通信工程研究所

考試科目：計算機組織與作業系統　　考試日期：0205，節次：1

※ 考生請注意：本試題不可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1.(10%)

(a)What is the multilevel feedback queues scheduling algorithms.

(b)Describe the parameters which are used to define the multilevel feedback queues scheduler.

2.(10%)

(a)Explain the role of the init process on UNIX and Linux systems in regard to process termination.

(b)Including the initial parent process, how many processes are created by the program shown in Figure 1?

```
#include <stdio.h>
#include <unistd.h>
Int main()
{
    int i;
    for (i=0; i<4;i++)
        fork();
    return 0;
}
```

Figure 1.

3.(10%)

Why do Solaris, Linux, and Windows 2000 use spinlocks as a synchronization mechanism only on multiprocessor systems and not on single-processor systems?

4.(10%)

Most systems allow a program to allocate more memory to its address space during execution. Allocation of data in the heap segments of programs is an example of such allocated memory. What is required to support dynamic memory allocation in the following schemes?

(a) Contiguous memory allocation

(b) Pure segmentation

(c) Pure paging

5.(10%)

What is the copy-on-write feature, and under what circumstances is its use beneficial? What hardware support is required to implement this feature?

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6. (5 %) When a cache write miss occurs, the missing block is read in first and then the write is performed in the cache. What is the name for this write policy?

7. (5 %) What is the name for machines that can issue multiple independent instructions in a single clock cycle?

8. (5 %) What is the name describing the event that a page is not found in the main memory?

9. (5 %) And what is the name describing the event that an address translation is not found in the TLB?

10. (10 %) Write down 5 exceptions that may occur in a processor.

11. (20 %) Design a single-cycle implementation of processor for the MIPS-like instruction: lw Rt , offset (Rs). Answer the following questions:
    (a). Show the processor datapath for the load instruction.(10%)
    (b). Assume that the first step fetches an instruction from the memory using PC; also finally the PC is incremented by 4. Draw a relative timing diagram of one clock cycle showing (1) at about what time, the PC+4 is valid, (2) at what time, the PC is updated, (3) at what time, the instruction fetched is obtained. State your assumptions.(10%)