國立成功大學 107 學年度碩士班招生考試試題

系　　所：電機工程學系

考試科目：計算機組織

考試日期：0205，節次：2

※ 考生請注意：本試題不可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

Fill in the most appropriate answer for Problem 1 to 4.

1. (10 pts). A direct mapped cache has 32 lines and each line is 16 bytes. The size of this cache is (a)_____ bytes. If the cacheable memory is 256MB, the tag size of this cache is (b) _____ bytes. To access this cache, the index field uses (c)_____ bits of the address. Will address 35 and 98 be mapped to the same line or not? (d) _____ (Yes or No). To which set does address 127 map? (e) _____.
2. (10 pts). True or false. Both DRAM and SDRAM do not use clock when accessing them. (a) _____. What is S in SDRAM? (b) _____. DDR is the short for (c) _____. Generally an address accessing a DRAM chip composes of the (d) _____ address bits, the (e) _____ address bits, and the bank address bits.
3. (10 pts). For a data write, which byte-lanes of the data bus carry valid data is identified by the (a) _____ signals used to trigger the corresponding byte-sections of memory to receive the data. 32-bit address lines can address (b) _____ GB memory space given each location has one byte.
4. (10 pts). CPU execution time = Instruction count × (a) _____ × clock cycle time. RISC is short for (b) _____.

Choose the most appropriate answers for the following multiple choice problems. Each question may have more than one answer. 10 points each, no partial point, no penalty.

5. (10 pts) Which of the following logic devices are state elements?
   a. flip flop　b. register　c. ALU　d. SRAM memory　e. program counter
   f. NAND gate　g. MUX

6. (10 pts) Which of the following address are misaligned for a 32-bit word? (N is an integer, >= 0)
   a. 4N + 2　b. 4N + 3　c. 8N + 4　d. 4N　e. 8N + 1.

7. (10 pts) Which of the following is (are) true for hazards in a MIPS five-stage pipelined processor?
   (a) Considering two instructions i and j, with i occurring before j, j tries to read a source before i writes it, so j incorrectly gets the old value. This is a read after write hazard.
   (b) Load-use data hazard is RAW hazard.
   (c) EX/MEM hazard: if (EX/MEM.RegWrite and (EX/MEM.RegisterRd ≠ 0) and (EX/MEM.RegisterRd = ID/EX.RegisterRs)), this detects the Rd dependency of the operand reading instruction in the EXE stage.
   (d) EX/MEM hazard: if (EX/MEM.RegWrite and (EX/MEM.RegisterRd ≠ 0)

and (EX/MEM.RegisterRd = ID/EX.RegisterRs)), this detects the Rt dependency of the operand reading instruction in the ID stage.

(e) EX/MEM hazard: if (EX/MEM.RegWrite and (EX/MEM.RegisterRd ≠ 0) and (EX/MEM.RegisterRd = ID/EX.RegisterRt)), this detects the Rt dependency of the operand reading instruction in the EXE stage.

8. (10 pts) Which of the following is (are) true for virtual memory system?
   (a) A TLB exception can be triggered by the instruction fetch operation or execution of a load or store instruction.
   (b) TLB caches the most recently used instruction and data.
   (c) A page table is stored in the main memory and shared among the programs in execution.
   (d) The page table lookup may fail if there is no translation available for the virtual address, meaning that virtual address is invalid. This will typically occur because of a programming error, and the operating system must take some action to deal with the problem. On modern operating systems, it will cause a segmentation fault in the offending program.
   (e) The page table lookup may also fail if the page is currently not resident in physical memory. This is a page fault.

9. (10 pts) Which of the following is (are) true as a processor is booted from power-on?
   (a) The processor asks the OS to give the first instruction address for booting.
   (b) The first instruction is fetched using the program counter value given from the power supply.
   (c) The first instruction is fetched by the processor using the address specified in the stack pointer.
   (d) The processor has an initialized PC value upon power-on reset.
   (e) The processor loads in the PC from ROM upon power-on reset.

10. (10 pts) Which of the following is (are) true about instruction set architecture (ISA)?
   (a) An instruction set architecture (ISA) is an abstract model of a computer.
   (b) A realization of an ISA is called an implementation.
   (c) An ISA permits multiple implementations that may vary in performance, physical size, and monetary cost because the ISA serves as the interface between software and hardware.
   (d) Software that has been written for an ISA can run on different implementations of the same ISA.
   (e) RISC-V and ARM are both RISC-type ISA and use the same instructions set architecture.