1. Fig.1 shows a CMOS inverter gate and its transfer curve.

   $| V_{TN} | = | V_{TP} | = 1$ V, $K_n = 4K_p = 100$ μA/V^2.

   (a) Find V_H, V_1, V_2, V_T.

   (b) A 100 KHz clock signal (High level 5 V, Low level 0 V) is applied to the input of CMOS inverter gate, and the output load of the gate is a 10 pF capacitor. Calculate the average power consumption of the gate.

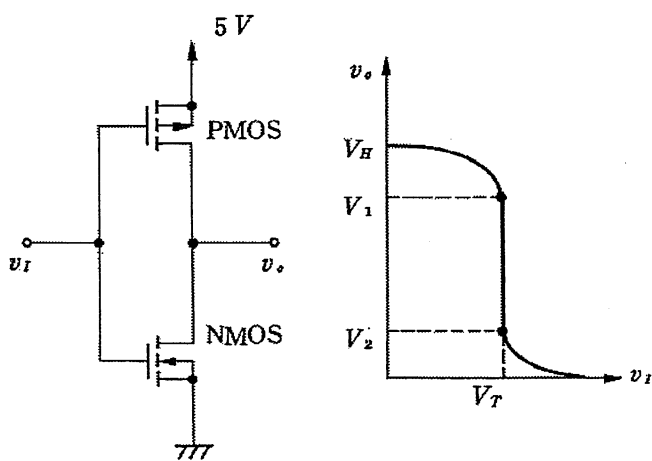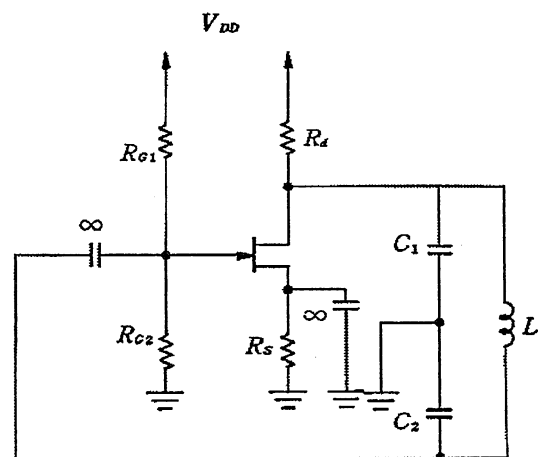   (c) Sketch the circuit diagram of a CMOS NAND gate with 2 input terminals.

Fig.1

Fig.2

2. The circuit is shown in Fig.2, assume that the input impedance of the FET amplifier is very large and the FET is adequately characterized by an ideal voltage-controlled current-source model.

   Find the frequency of oscillation ω_o and the minimum gain ($g_m R_d$) required for the circuit to oscillate.

〈背面繼續〉

註：本次考試 不可以參考自己的書籍及筆記；不可以使用字典；不可以使用計算器。

3. The diode is "turned on" and "turned off" at $t = 0$ and $t = t_1$, as shown in Fig.3. What is the variation of current i as function of time?

4. A bipolar transistor is used in the circuit of Fig.4.
   Given that $V_{CC} = 22.5$ V, $R_C = 5.6$ kΩ, $R_e = 1$ kΩ, $R_2 = 10$ kΩ and $R_1 = 90$ kΩ, $\beta = 50$, $C_b = 1$ μF.
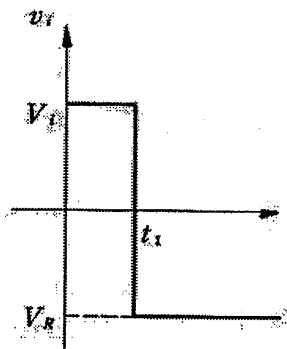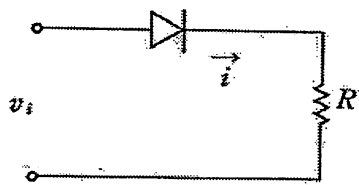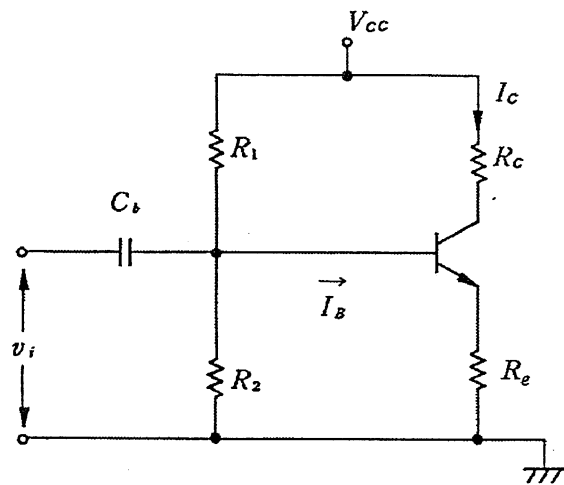   Find I_C and I_B.

Fig.3　　　　　　　　　Fig.4

5. For the comparator in Fig.5, determine the maximum value of R_f that will ensure correct switching (no chatter) of the zero crossing point.
   Assume that $V_Z = 10$ V, $V_D = 0.7$ V, $V_S = (5\ sim\omega_o t\ +\ 0.05\ sim100\omega_o t)V$.

Fig.5