逢甲大學100學年度碩士班招生考試試題 編號：076 科目代碼：335

科目	數位電路(含邏輯設計)	適用系所	電子工程學系電路與系統組	時間	100分鐘

※請務必在答案卷作答區內作答。 共 3 頁第 1 頁

The "V_{OUT} vs. V_{IN} VTC curve" analysis is very important for the discussion of the static performance of a digital circuit. Let us make a test of this fundamental skill by means of the following two basic inverter-modules of both the BJT and the CMOS technologies.

1、The current gain of the transistor in Fig.1 is $\beta = 100$, $V_{BE(ACT)} = 0.7$ V, $V_{BE(SAT)} = 0.8$ V, and $V_{CE(SAT)} = 0.2$ V. Plot the V_{OUT} vs. V_{IN} VTC curve of this circuit. Note ： You have to indicate the breakpoints and to annotate the slopes of the curve. (10 pt.s)

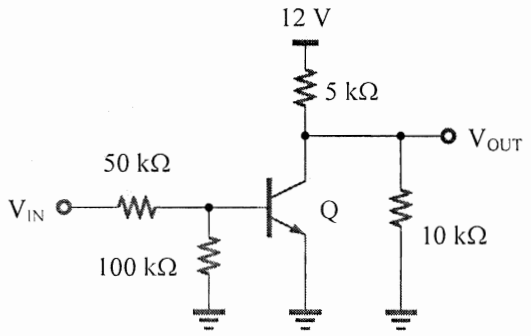
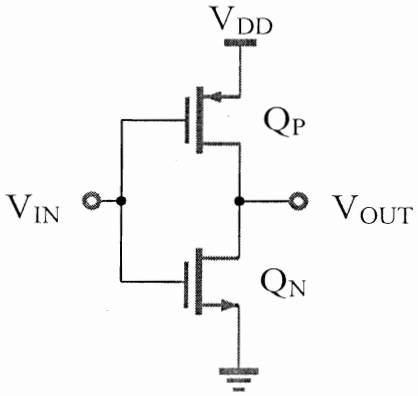


Fig. 1

2、A CMOS inverter shown in Fig.2(A) with NMOS-FET Q_N parameters (K_N , $(W/L)_N$, and V_{TN}) and PMOS-FET Q_P parameters (K_P , $(W/L)_P$, and V_{TP}) is a basic structure for the CMOS digital circuit. Neglecting the effect of the channel-length modulation of both MOSFETs (Q_N and Q_P), the V_{OUT} vs. V_{IN} VTC curve of this inverter is shown in Fig.2(B). Please answer the following questions.



Q_N ：(K_N , $(W/L)_N$, and V_{TN})
Q_P ：(K_P , $(W/L)_P$, and V_{TP})

Fig. 2(A)

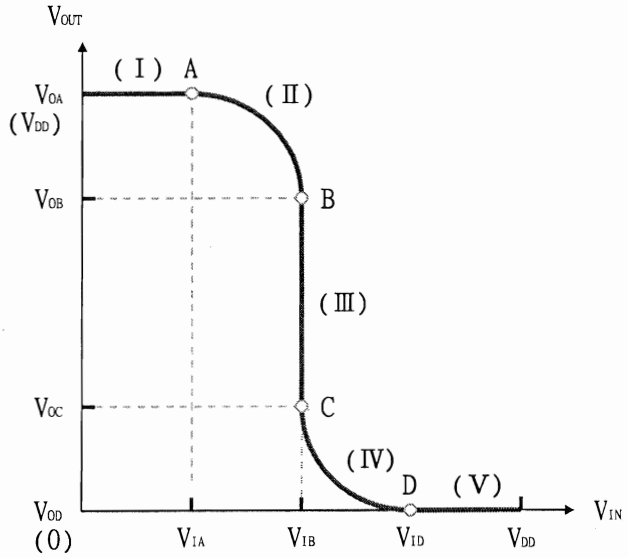


Fig. 2(B)

(1) Indicate the operation regions of both MOSFET using annotations (OFF , SAT, and Ω regions) within each field labeled by the (Ⅰ , Ⅱ, Ⅲ, Ⅳ, Ⅴ) characters. (5 pt.s)

	Ⅰ	Ⅱ	Ⅲ	Ⅳ	Ⅴ
Q_N					
Q_P					

(2) Analyze and express the breakpoints B(V_{IB}, V_{OB}), C(V_{IC}, V_{OC}) of the VTC curve using the parameters of Q_N and Q_P. (10 pt.s)

(3) The noise margins NM_H and NM_L are defined by $NM_H \equiv V_{OH} - V_{IH}$, and $NM_L \equiv V_{IL} - V_{OL}$. As we know that the $V_{OH} = V_{DD}$ and $V_{OL} = 0$ V .Describe briefly (don't need to calculate) how to analyze the V_{IL} , and V_{IH} of this CMOS inverter. (5 pt.s)

(4) What is the meaning of "a symmetric-design", and explain how to deal with it. (5 pt.s)

(5) Changing the relative ratio (K_N / K_P) of the aspect-ratio of the MOSFETs Q_N and Q_P , what will be happened on the VTC curve, and explain the reasons why. (5 pt.s)

(6) Using this inverter circuit, explain "the dynamic power dissipation ; $P_{D(dynamic)}$" and "the short-circuit current; I_{SC}" of a CMOS digital circuit. (5 pt.s)

(7) For a correct inverter-operation , what is the necessary condition of the supply voltage V_{DD}. How comes ? (5 pt.s)

3. 5% Please minimize the following expression:

$\overline{B}\overline{C}\overline{D} + \overline{A}B\overline{C}\overline{D} + AB\overline{C}\overline{D} + \overline{A}\overline{B}CD + \overline{A}BCD + \overline{A}\overline{B}C\overline{D} + \overline{A}BC\overline{D} + ABC\overline{D} + A\overline{B}C\overline{D}$

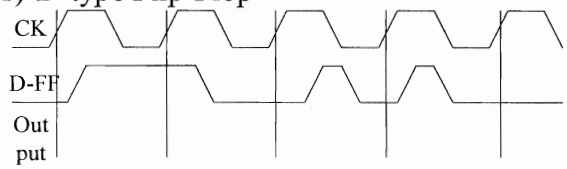
4. 5%Please design and make the logic circuit as simple as possible of Y(A, B, C, D)=Σm(7,9,10,11,12,13,14,15)..

5. 5%Please design a logic gate circuit can implement the function of a 4-1 Multiplexer.

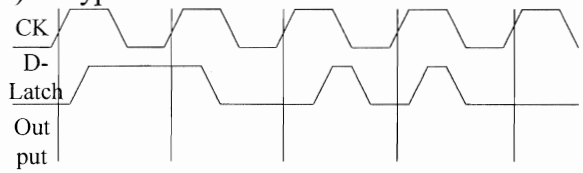
6. 5%Please design a logic gate circuit can implement the function of a 4-2 Encoder.

7. 10%Please draw the output waveforms for the follows logic device

(1) D-type Flip-Flop



(2) D-type Latch



8. 10%Please use the D-FF to design a **Synchronous counter** with the counting sequence of 0->1->3->5->7->0.

9. 10%Please use the JK-FF to design a **Asynchronous counter** with the counting sequence of 0->7->6->5->4->3->2->1->0