中原大學 100 學年度 碩士班 入學考試

3 月 19 日 10:30~12:00　　電子工程學系晶片設計組

誠實是我們珍視的美德，
我們喜愛「拒絕作弊，堅守正直」的你！

科目：數位電路　　（共 1 頁第 1 頁）

□可使用計算機，惟僅限不具可程式及多重記憶者　　☑不可使用計算機

1. [10%] **Simplify** the following Boolean expressions to a **minimum** number of **literals**:
   (a) xyz' + x'yz + xyz + x'yz'
   (b) A'B(D' + C'D) + B(A + A'CD)

2. [10%] Write a **truth table** for a **half adder**. Then use logic gates to **implement** the half adder.

3. [15%] Design a combinational circuit with **three inputs** and **one output**. The output is **1** when the binary value of the inputs is **less than 3**. Otherwise the output is 0. Show the design process and **plot** the circuit.

4. [10%] Design a **5-to-32-line decoder** with four 3-to-8-line decoders with enable and one 2-to-4-line decoder. Use block diagrams for the components.

5. [10%]
   (a) Write the **truth table** (or characteristic table) of a **J-K** flip-flop.
   (b) Write the **excitation table** of a **S-R** flip-flop.

6. [20%] A sequential circuit has two D flip-flops *A* and *B*, two inputs *x* and *y*, and one output *z*. It is specified by the following next-state and output equations:
   $$A^+ = Ax + Bx, \quad B^+ = A'x, \quad z = (A + B)x'.$$
   (a) Draw the **logic diagram** of the circuit.
   (b) List the **state table** for the circuit.
   (c) Draw the corresponding **state diagram**.

7. [25%] A counter is counting in the repeated sequence 000→ 001→ 011→ 010→ 110→ 100→ 000→….
   (a) **Plot** its state diagram.
   (b) Use **J-K** flip-flops to **implement** it.
   (c) Use **Verilog** or **VHDL** language to describe this circuit.