1. (**15 points**)
Assume that logical address is 32-bits wide and physical address is 36-bits wide. If the mapping is done by two-level paging while both levels use 10 bits,
   (a) (5 points) what is the size of a page?
   (b) (10 points) how many entries are there in the first level page table and second level page table?

2. (**10 points**)
Demand paging is often used to implement virtual memory. It is based on the assumption that OS will load pages when they are needed. But how does OS know the need of a program?

3. (**25 points, 5 points for each**)
Answer Yes or No for following questions.
   (a) Context-switch does affect the performance of cache.
   (b) The LRU page replacement algorithm always performs well.
   (c) For accessing a regular file on a disk, the ***write*** operations are possibly much faster than the ***read*** operations.
   (d) The name of a file, in UNIX implementation, is stored in its inode.
   (e) In order to save power, some system will turn off the screen or slow down the CPU when it is idle. This operation is initiated by kernel.

4. (**18 points**)
   (a) (12 points) Explain the memory wall problem, what memory hierarchy is, and how memory hierarchy help ease the memory wall problem.
   (b) (6 points) If the time of retrieving one word from the main memory was the same as the time of executing one instruction, does the memory wall problem still exist? Explain your reason.

5. **(24 points)**
   (a) (12 points) Explain the three kinds of pipeline hazard.
   (b) (4 points) Assume that we have a CPU with *n*-stage pipeline, and the execution time of each pipeline stage is the same. Compared to the CPU with single-cycle datapath, how much speedup can we get under ideal pipeline, i.e. no pipeline stalls at all?
   (c) (8 points) Is utilizing more pipeline stages good for performance? Does more pipeline stages need more cost? What kind of extra cost does a pipeline stage need?

6. **(8 points)**
   The equation of calculating CPU time is CPU time = CPI * IC * Cycle_time, where CPI is Clock Cycle per Instruction, and IC is instruction count.
   (a) (4 points) How could a compiler help improve performance?
   (b) (4 points) How can we reduce CPI?