國立彰化師範大學106學年度碩士班招生考試試題

系所：電子工程學系(乙組選考乙)、資訊工程學系(選考丁)、資訊工程學系積體電路設計碩士班(選考丙)　　科目：計算機組織

☆☆請在答案紙上作答☆☆　　

1. Consider the following C codes (procedure swap(v, j) swaps v[j] and v[j+1]). (5%+10%)

```
void sort ( int v[ ], int n )
{   int i, j;
    for ( i=0; i<n; i+=1) {
      for ( j=i-1; j>=0 && v[j]>v[j+1]; j-=1) { swap( v, j );}
                    }
}
```

   (a) Assume n=5 and v[0] to v[4] are initially 3, 5, 1, 9, 7. List the temporary results of v[ ] at the end of i=0,1,2,3,4, respectively. In this example, how many swaps are actually invoked totally?
   (b) Implement the outer loop (i loop) with MIPS assembly language (Assume i is in $s0, j is in $s1, v is in $s2, and n is in $s3).

2. Transform the decimal real into IEEE754 single precision and vice versa. (10%)
   (a) -1.625 (decimal real)　note: use hex format to shorten your answer
   (b) C0A00000 (IEEE754 single precision in hex)

3. Consider 2 different implementations P1 and P2 of the same Instruction Set Architecture (ISA). There are 4 classes of instructions A, B, C and D, as shown in the following table. (15%)

	Clock rate	CPI_A	CPI_B	CPI_C	CPI_D
P1	1.5 GHz	1	2	3	4
P2	2GHz	2	2	2	2

   (a) Given a program with10^6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C and 20% class D, which implementation is faster?
   (b) What is the global CPI for each implementation?
   (c) Find the clock cycles required in both cases.

4. Explain the following terminologies/registers based on your understanding. (10%)
   (a) assembler
   (b) IEEE double precision
   (c) $sp
   (d) $ra
   (e) pseudo-instruction.

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5. Explain the following terminologies. (16%)
   (a) Program counter (PC)
   (b) Exception program counter (EPC)
   (c) Cache miss
   (d) Page fault

6. What are the four steps in executing a MIPS instruction? (8%)

7. Explain the four-step process in handling an instruction cache miss. (10%)

8. For the single-cycle design in Fig. 1, determine what instructions (**add**, **lw**, **sw**, or **beq**) will be affected and cannot execute correctly if some functional unit is removed. Fill in the blanks in Table 1 with a letter "X" if the corresponding instruction is affected. (16%)

Table 1

Unit	add	lw	sw	beq
"Sign-extend" removed				
"Shift left 2" removed				
"Mux A" removed				
"Mux B" removed				

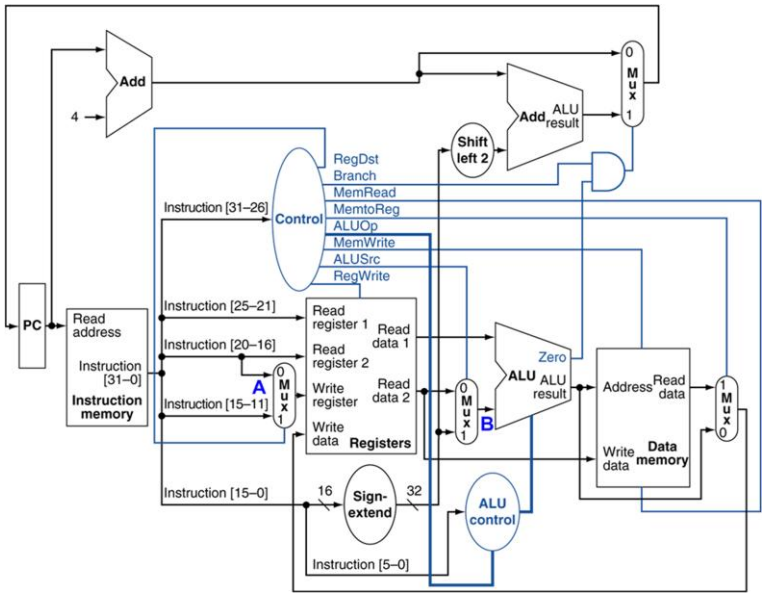

Fig. 1