# 國立臺灣師範大學 106 學年度碩士班招生考試試題

科目：計算機系統　　適用系所：資訊工程學系

注意：1.本試題共 3 頁，請依序在答案卷上作答，並標明題號，不必抄題。2.答案必須寫在指定作答區內，否則依規定扣分。

一、(6 分) Convert the following hexadecimal numbers to binary numbers:

（一）(3 分) $3A01_{hex}$

（二）(3 分) $1FC6_{hex}$

二、(10 分) Consider the MIPS code sequence shown below:

```
LW    R1,20(R12);      R1 ← MEM[R12+20]
LW    R2,24(R12);      R2 ← MEM[R12+24]
SUB   R3,R2,R1;        R3 ← R2-R1
ADD   R4,R8,R3;        R4 ← R8+R3
LW    R10,28(R12);     R10 ← MEM[R12+28]
ADD   R5,R10,R4;       R5 ← R10+R4
SW    R5,32(R12);      MEM[R12+32] ← R5
LW    R11,36(R12);     R11 ← MEM[R12+36]
```

The code sequence is executed by a MIPS CPU with separate instruction and data memories. Suppose the execution of the code sequence takes 16 clock cycles. The clock cycle time is 1ns.

（一）(2 分) Find the clock cycles per instruction (CPI) of the code sequence,

（二）(2 分) Find the CPU time of the code sequence,

（三）(2 分) Find the number of accesses to the instruction memory,

（四）(2 分) Find the number of accesses to the data memory.

（五）(2 分) Identify all the instructions where the ALU of the CPU is used for the computation of memory addresses for data accesses.

三、(12 分) Consider a cache with 64 blocks, and a block size of 64 bytes.

（一）(3 分) Suppose the cache is direct mapped. What cache block number does byte address 16000 map to?

（二）(3 分) Suppose the cache is direct mapped. What cache block number does byte address 32128 map to?

（三）(3 分) Suppose the cache is 2-way set associative. How many sets are there in the cache?

（四）(3 分) Suppose the cache is 2-way set associative. What cache set number does byte address 16000 map to?

四、(10 分) Consider a MIPS processor with five-stage (i.e., IF, ID, EX, MEM, WB) pipeline. Suppose the processor has separate instruction and data memories. The hazard detection and forwarding units are also employed. Assume there is no structural hazard. There is also no cache miss. Find the number of clock cycles required by the pipeline for the execution of each of the following sequences.

（一）(5 分)

```
ADD   R3,R2,R1;        R3 ← R2+R1
ADD   R4,R10,R3;       R4 ← R10+R3
```

（二）(5 分)

```
LW    R6,12(R4);       R6 ← MEM[R4+12]
ADD   R8,R10,R6;       R8 ← R10+R6
ADD   R12,R6,R8;       R12 ← R6+R8
```

五、(12 分) Consider a two-level cache. Suppose the hit time of the L1 cache is 1 clock cycle. The local miss rate of the L1 cache is 25%. The hit time of the L2 cache is 6 clock cycles. The local miss rate for L2 is 4%. The L2 is connected to main memory. It will take 250 clock cycles to access a cache block from main memory.

（一）(4 分) Compute the average memory access time of L2 cache (in clock cycles),

（二）(4 分) Compute the miss penalty for L1 cache (in clock cycles),

（三）(4 分) Compute the average memory access time of L1 cache (in clock cycles).

六、(9 分) What are the three general methods used to pass parameters to operating systems during system calls?

七、(10 分) Illustrate a diagram to show the process states and state transitions in the lifecycle of processes.

八、(9 分) Suppose multiple threads are used in a web server to serve concurrent requests from multiple devices and accounts.

（一）(3 points) What is a thread pool model?

（二）(6 points) How may a thread pool model limit the resources used by the

web server to serve the concurrent requests?

九、(15 分) Consider the following processes. Please illustrate the Gantt Chart and determine the average waiting time of the execution for following short-term scheduling algorithms.

| Process | Burst time | Arrival time |
|---|---|---|
| P1 | 9 | 0 |
| P2 | 3 | 4 |
| P3 | 7 | 2 |
| P4 | 5 | 6 |

（一）(5 分) Preemptive Shortest-Job-First.

（二）(5 分) First-Come, First-Served.

（三）(5 分) Round-Robin.

十、(7 分) Please answer following questions about memory management.

（一）(3 分) What is the three stages where address binding of instructions and data to memory addresses can happen?

（二）(4 分) What is the difference between internal and external fragmentation?