國立中山大學106學年度碩士暨碩士專班招生考試試題

科目名稱：計算機結構【資工系碩士班甲組、乙組】　　題號：434001

※本科目依簡章規定「不可以」使用計算機(問答申論題)　　

NOTE: If some questions are unclear or not well defined to you, you can make your own assumptions and state them clearly in the answer sheet.

1. (5% total) True or False. (If the statement is false, please explain the answer shortly)
   ____ 1.1 (1%) Increasing the block size of a cache is likely to take advantage of temporal locality.
   ____ 1.2 (1%) Increasing the page size tends to decrease the size of the page table.
   ____ 1.3 (1%) Virtual memory typically uses a write-back strategy, rather than a write-through strategy.
   ____ 1.4 (1%) If the cycle time and the CPI both increase by 10% and the number of instruction decreases by 20%, then the execution time will remain the same.
   ____ 1.5 (1%) In uniform memory access (UMA) designs, all processors use the same address space.

2. (10% total) Server farms such as Google and Yahoo! Provide enough computer capacity for the highest request rate of the day. Imaging that most of the time these servers operate at only 60% capacity. Assume further that the power does not scale linearly with the load; that is, when the servers are operating at 60% capacity, they consume 90% of maximum power. The servers could be turned off, but they would too long to restart in response to more load. As new system has been proposed that allows for a quick restart but requires 20% of the maximum power while in this "barely alive" state.
   2.1 (5%) How much power saving would be achieved by turning off 60% of the servers?
   2.2 (5%) How much power saving would be achieved by placing 60% of the servers in the "barely alive state?

3. (20% total) A multicycle CPU has three implementations. The first one is a 5-cycle IF-ID-EX-MEM-WB design running at 4.8GHz, where load takes 5 cycles; store/R-type 4 cycles and branch/jump 3 cycles. The second one is a 6-cycle design running 5.6GHz, with MEM replaced by MEM1 and MEM2. The third is a 7-cycle design running at 6.4GHz, with IF further replaced by IF1 and IF2. Assume we have an instruction mix: load 26%, store 10%, R-type 49%, branch/jump 15%.
   3.1 (10%) Do you think it is worthwhile to go for the 6-cycle design over the 5-cycle design?
   3.2 (10%) How about the 7-cycle design over the 6-cycle design, is it worthwhile?

4. (15% total) Identify all of the data dependencies in the following code running in a 5-stage pipelined MIPS CPU. Which dependencies are data hazards that will be resolves via forwarding? Which dependencies are data hazards that will cause a stall?

Line	Instructions
1	add $3 $4 $2
2	sub $5 $3 S1
3	lw $6 200($3)
4	add $7 $3 $6

5. (10% total) For a system with 32-bit address, the CPU uses a 4-way set associate cache with block size of 16 bytes. The cases has 1024 entries in total
   5.1 (5%) Determine the tag size for each block.
   5.2 (5%) Assume each block requires 2 extra valid bits. What is the size of the cache memory?

背面有題

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6. (20% total) Given the following datapath for the single-cycle implementation of a computer and the definition of its instructions:

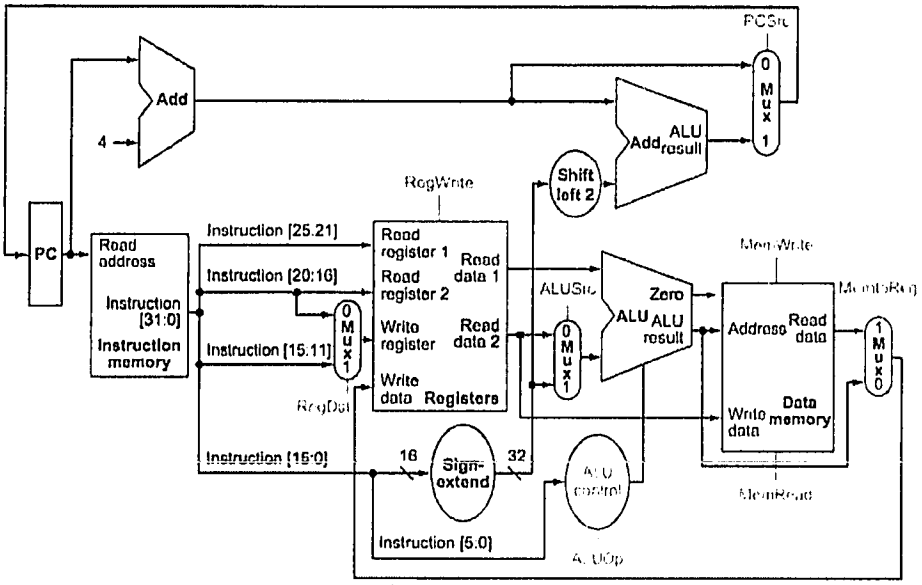

Figure 1.

add $rd $rs $rt
lw $rt addr($rs)
sw $rt addr($rs)
beq $rs $rt addr

Assume that the instructions are fixed length and the operation time for the major functional units in this implementation are as follows:

- Memory units: 2ns
- ALU and adders: 2ns
- Register file (read or write): 1ns
- Multiplexers, control unit, PC accesses, sign extension unit, and wires: no delay

Please compute the required time for each instruction and explain why.

7. (10% total) The following series of branch outcomes occurs for a single branch in a program. T means the branch is taken; N means the branch is not taken.
T T T N N T T T
How many instances of this branch instruction are mis-predicted with a 1-bit and 2-bit local branch predictor, respectively? Assume the Branch History Table (BHT) are initialized to the N state. You may assume that this is the only one branch in this program.

8. (10% total) A computer whose processes have 1024 pages in their address spaces keeps its page tables in memory. The overhead required for reading a word from the page table is 500 ns. In order to reduce the overhead, the computer has Translation Lookaside Buffer(TLB), which holds 32 (virtual page, physical page frame) pairs, and can do a look up in 100 ns. What hit rate is needed to reduce the mean overhead to 200 ns?