國立中山大學106學年度碩士暨碩士專班招生考試試題

科目名稱：計算機結構【電機系碩士班己組】　　題號：431007

※本科目依簡章規定「可以」使用計算機（廠牌、功能不拘）（問答申論題）　　

[Problem 1] (20%) Terminology Explanation

(a) Pipeline Processing (b) Superscalar Processor (c) RISC (d) GPGPU

[Problem 2] (20%)

Suppose we are considering a change to an instruction set. The base machine is a load-store machine. Measurements of the load-store machine showing the instruction mix and clock cycle counts per instructions are given in the following table:

Instruction Type	Frequency	Clock Cycle Count
ALU Operations	40%	1
Loads	25%	2
Stores	15%	2
Branches	20%	2

Let's assume that 30% of the ALU operations directly use a loaded operand that is not used again. We propose adding ALU instructions that have one source operand in memory. These new register-memory instructions have a clock cycle count of 2. Suppose that the extended instruction set increases the clock cycle count for branches by 1, but it does not affect the clock cycle time. Would this change improve CPU performance? Explain your answer.

[Problem 3] (20%) A set associative cache has a block size of four 32-bit words and a set size of 4. The cache can accommodate a total of 256K words. The main memory size that is cacheable is 1024M * 32 bits. Design the cache structure and show how the processor's addresses are interpreted.

[Problem 4] (20%) Given the 8-bits adder (named Add8), the 2-to-1 8-bits multiplexers (named MUX8_2to1) and the basic gates such as NOT, AND, OR, NAND, and NOR, you are asked to design an ALU in function block diagrams, which must match the following requirements:

(1) Support add, sub, and sgt (set on great than) functions. Their operation selection bits (op_sel) are as follows: add(00), sub(10), sgt(11),

(2) Report the result status in sign, zero, overflow, and carry bits.

[Problem 5] (20%) Use the following code fragment:

```
Loop:   LW      R1, 0(R2)
        ADDI    R1, R1, #2
        SW      0(R2), R1
        ADDI    R2, R2, #5
        SUB     R4, R3, R2
        BNEZ    R4, Loop
```

Assume the initial value of R3 is R2+100. Use the five-stage instruction pipeline (IF, DEC, EXE, MEM, WB) and assume all memory accesses are one cycle operation. Furthermore, branches are resolved in MEM stage.

(a) (10%) Show the timing of this instruction sequence for the five-stage instruction pipeline with normal forwarding and bypassing hardware. Assume that branch is handled by predicting it has not taken. How many cycles does this loop take to execute?

(b) (10%) Assuming the five-stage instruction pipeline with a single-cycle delayed branch and normal forwarding and bypassing hardware, schedule the instructions in the loop including the branch-delay slot. You may reorder instructions and modify the individual instruction operands, but do not undertake other loop transformations that change the number of op-code of instructions in the loop. Show a pipeline timing diagram and compute the number of cycles needed to execute the entire loop.