國立成功大學 106 學年度碩士班招生考試試題

系　　所：電腦與通信工程研究所

考試科目：計算機組織與作業系統　　考試日期：0214，節次：1

※ 考生請注意：本試題不可使用計算機。　請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

1. What is a semaphore and write two short methods that implement the simple semaphore wait() and signal() operations on global variable S. (10%)

2. Briefly describe the segmentation memory management scheme. How does it differ from the paging memory management scheme in terms of the user's view of memory? (10%)

3. Explain the difference between programmed I/O and interrupt driven I/O. (10%)

4. (a) What is a multilevel queue scheduling algorithm. (5%)
   (b) Consider a system implementing multilevel queue scheduling. What strategy can a computer user employ to maximize the amount of CPU time allocated to the user's process? (5%)

5. Consider the "exactly once" semantic with respect to the RPC mechanism. Does the algorithm for implementing this semantic execute correctly even if the ACK message sent back to the client is lost due to a network problem? Describe the sequence of messages, and discuss whether "exactly once" is still preserved. (10%)

6. For a MIPS-like 5-stage pipelined processor,
   a. Explain how the processor handles the control hazard for beq rs, rt, loop instruction. (Assume that non-taken prediction is used; state your assumptions for the implementation of the beq instruction), (10%)
   b. In a MIPS-like 5-stage pipelined processor, what is a load-use hazard? (5%)
   c. How to handle this load-use hazard in the pipeline? (5%)
   d. Assume that an exception handling unit is placed at the MEM stage of the pipeline. What is the precise interrupt PC? (5%)
   e. Define precise interrupt. (5%)

7. Design a DTLB and data cache system. Assume both the virtual address and physical address are 32 bits. The page size is 4KB. The DTLB uses 4-way set associative structure and has a total of 32 entries. The data cache is physically addressed; cache size 32KB, direct-mapped, line size 32 bytes.
   a. Show the integrated design of the DTLB and the data cache. (10%)
   b. Show the integration of this sub-memory system into a 5-stage processor pipeline. (10%)