1. (a) Please draw the physical structure of the NMOS transistor and explain how it can be used as a switch in digital circuits. When the body effect is considered, explain how the NMOS switches effected. (6%)

   (b) Draw the current-voltage characteristics of an NMOS transistor. Mark the operation regions in your plot and explain how an NMOS transistor works as an amplifier. (6%)

2. Assume that the characteristics of the diodes in Fig. P2 can be modeled by a constant voltage, 0.6V, when they are conducting. Find the values of the labeled voltages and currents.(10%)

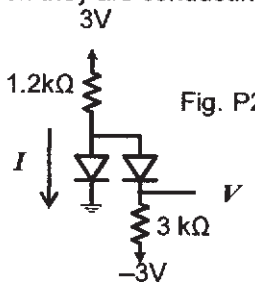

Fig. P2(a)

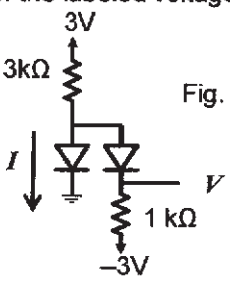

Fig. P2(b)

3. Fig. P3 shows a common-source amplifier with source degeneration resistance.
   (a) Let R_s = 0Ω and Ignore R_{G1} and R_{G2} for now. Plot the voltage transfer characteristic of this amplifier. (5%)
   (b) Assuming the NMOS is operating in saturation region, is the amplification linear? Please explain the reason. (3%)
   (c) Given V_{DD}=9V, V_t=1V, $\mu_n C_{OX}(W/L)$=1 mA/V², and λ=0, design proper DC bias for this amplifier to establish a dc drain current I_D = 0.5mA for linear amplification.(5%)
   (d) R_{sig} = 500Ω. Draw the small-signal model and calculate the small-signal gain of your design in (C). (5%)

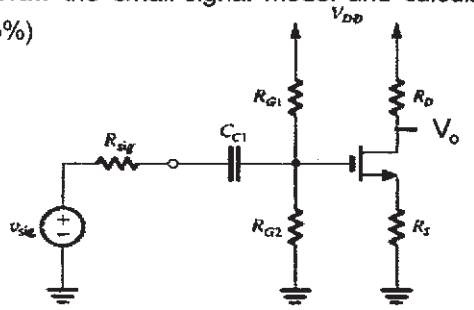

Fig. P3

4. Find I_{out} if I_{IN} = 80μA, R_2 = 4kΩ, $\mu_n C_{OX}$=160 μA/V², and $(W/L)_1=(W/L)_2$=16. Also, find the overdrive voltage of M_2, V_{ov2}. (10%)

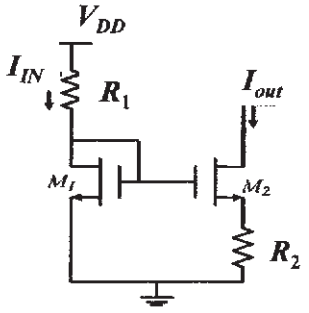

Fig. P4

5. (a) Sketch the general architecture of semiconductor memories and describe each functional block briefly. (5%)

   (b) A type of basic memory cell for EPROM is an enhancement type n-channel MOSFET with two gates made of polysilicon material (stacked-gate). Please describe the working principles of the EPROM using such stacked-gate memory cell. (10%).

6. A CMOS ring oscillator is designed as shown in Fig. P6. Do you think that the circuit in Fig .P6 will work properly? If your answer is "yes", please explain the reason in detail. Otherwise, redesign the circuit and describe the design principles in detail. (10%)

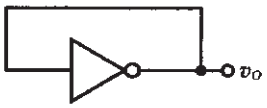

Fig. P6

7. (a) Please use small-signal π-model to derive the voltage gain of the cascode amplifier shown in Fig. P7. Assume that $g_{m1} \sim g_{m8}$ and $r_{o1} \sim r_{o8}$ represent the transconductance and output impedance of $M_1 \sim M_8$, respectively.(7%)

   (b) If M1 ~ M8 have the same (W/L) ratio of 40 and the cascode amplifier of Fig. P7 is fabricated with the following parameters: $\mu_n C_{OX} = 2\,\mu_p C_{OX} = 100\text{mA/V2}$, $\lambda_n = 0.1V^{-1}$, $\lambda_p = 0.2V^{-1}$, and $V_{tn}=|V_{tp}|=1V$. Please find the voltage gain with a tail current (I_s) of 1mA. (4%)

   (c) Please try to modify the cascode amplifier in Fig. P7 to boost the voltage gain. (4%)

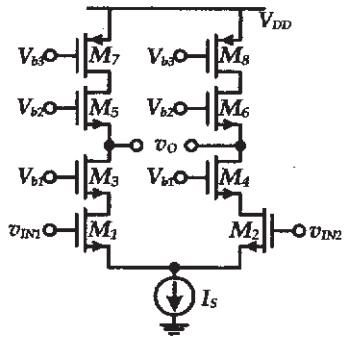

Fig. P7

8. The common-source amplifier is configured as the negative feedback loop with a frequency - independent β as shown in Fig. P8. Assume that (W/L) ratio of Q may vary by ±10% and λ of Q may decrease by 20%. What is the minimum loop gain necessary to guarantee that the close-loop gain increases by less than 5%. (10%)

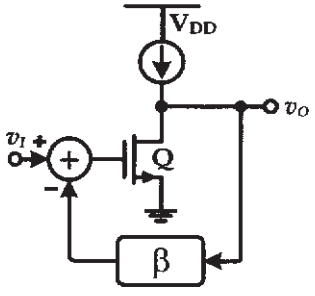

Fig. P8