1. (a) Please draw the physical structure of the NMOS transistor and explain how it can be used as a switch in digital circuits. When the body effect is considered, explain how the NMOS switches effected. (6%)

   (b) Draw the current-voltage characteristics of an NMOS transistor. Mark the operation regions in your plot and explain how an NMOS transistor works as an amplifier. (6%)

2. Assume that the characteristics of the diodes in Fig. P2 can be modeled by a constant voltage, 0.6V, when they are conducting. Find the values of the labeled voltages and currents.(10%)

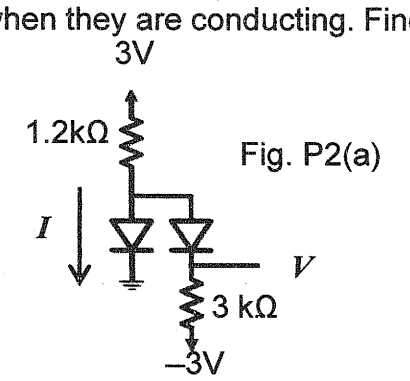


Fig. P2(a)

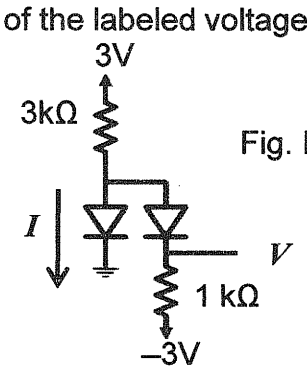


Fig. P2(b)

3. Fig. P3 shows a common-source amplifier with source degeneration resistance.

   (a) Let $R_s$ = 0Ω and Ignore $R_{G1}$ and $R_{G2}$ for now. Plot the voltage transfer characteristic of this amplifier. (5%)

   (b) Assuming the NMOS is operating in saturation region, is the amplification linear? Please explain the reason. (3%)

   (c) Given $V_{DD}$=9V, $V_t$=1V, $\mu_n C_{OX}(W/L)$=1 mA/V², and λ=0, design proper DC bias for this amplifier to establish a dc drain current $I_D$ = 0.5mA for linear amplification.(5%)

   (d) $R_{sig}$ = 500Ω. Draw the small-signal model and calculate the small-signal gain of your design in (C). (5%)

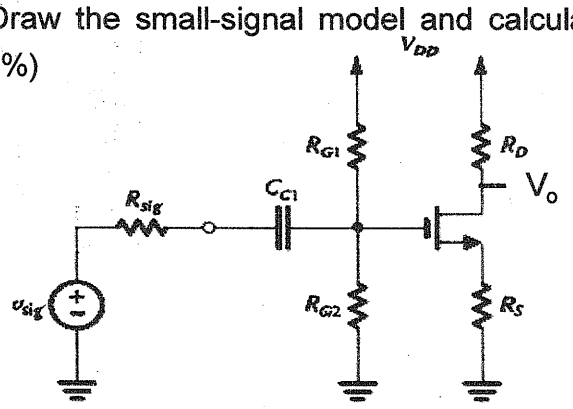


Fig. P3

4. Find $I_{out}$ if $I_{IN}$ = 80μA, $R_2$ = 4kΩ, $\mu_n C_{OX}$=160 μA/V², and $(W/L)_1=(W/L)_2$=16. Also, find the overdrive voltage of $M_2$, $V_{ov2}$. (10%)

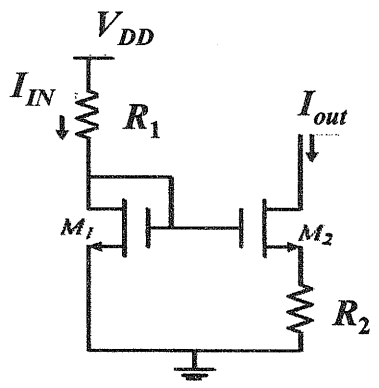


Fig. P4

5. (a) Sketch the general architecture of semiconductor memories and describe each functional block briefly. (5%)

(b) The sense amplifier shown in Fig. P5 is fabricated with the following parameters: $\mu_n C_{OX} = 2.5\mu_p C_{OX} = 100\mu A/V^2$, $V_{tn} = |V_{tp}| = 1V$, $V_{DD} = 5V$. In case of reading logic 1, assume that the storage cell provides a voltage increment in the Bit Line of $\Delta V(1) = 0.2V$ and the load capacitance of bit line ($C_{BL}$) is 2pF. Please determine the minimum (W/L) ratios for $M_1 \sim M_4$ to achieve 4ns accessing time ($v_B$ reach 4.5V). Assume $\mu_n C_{OX}(W/L)_n = \mu_p C_{OX}(W/L)_p$.(10%)

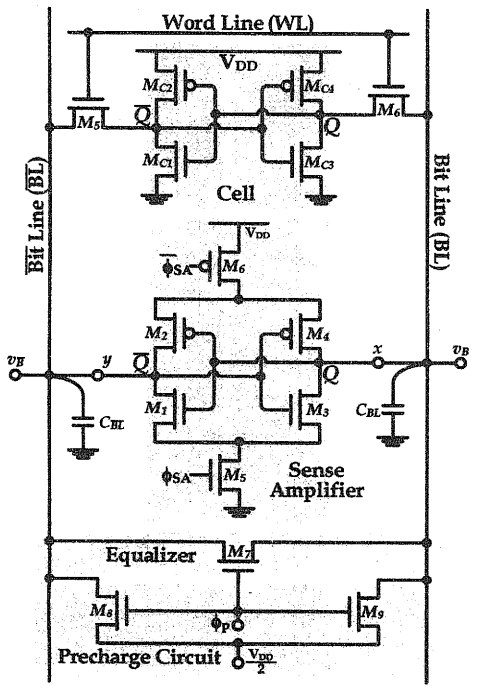


Fig. P5

6. (a) Please use small-signal $\pi$-model to derive the voltage gain of the cascode amplifier shown in Fig. P6. Assume that $g_{m1} \sim g_{m8}$ and $r_{o1} \sim r_{o8}$ represent the transconductance and output impedance of $M_1 \sim M_8$, respectively.(7%)

(b) If $M_1 \sim M_8$ have the same (W/L) ratio of 40 and the cascode amplifier of Fig. P6 is fabricated with the following parameters: $\mu_n C_{OX} = 2\mu_p C_{OX} = 100\mu A/V^2$, $\lambda_n = 0.1V^{-1}$, $\lambda_p = 0.2V^{-1}$, and $V_{tn} = |V_{tp}| = 1V$. Please find the voltage gain with a tail current ($I_s$) of 1mA. (4%)

(c) Please try to modify the cascode amplifier in Fig. P6 to boost the voltage gain. (4%)

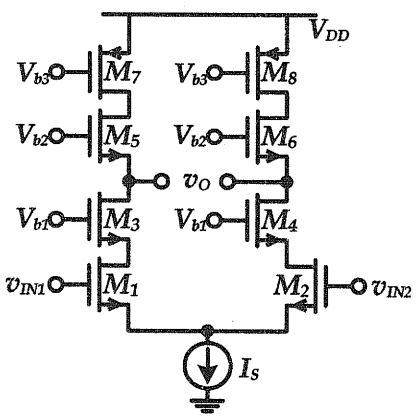


Fig. P6

7. A CMOS ring oscillator is designed as shown in Fig. P7. Do you think that the circuit in Fig .P7 will work properly? If your answer is "yes", please explain the reason in detail. Otherwise, redesign the circuit and describe the design principles in detail. (10%)

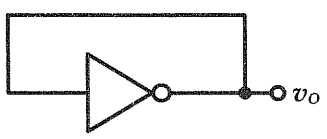


Fig. P7

8. An amplifier has a gain of $10^4$ at low-frequency and two poles at $10^3$ Hz and $10^5$ Hz. Now the amplifier is configured as a closed negative feedback loop with a frequency-independent feedback factor.

   (a) Find the value of feedback factor to result in two coincident close-loop poles, and also indicate the frequency. (5%)

   (b) What is the low-frequency gain corresponding to the situation in (a)? And what is the value of the closed-loop gain at the frequency of the coincident poles? (5%).