國立中山大學100學年度碩士班招生考試試題

科目：電子學【海下海物所碩士班選考】

1. (15%) For the circuit shown in Fig. 1, find the transfer function $T(s) = V_o(s) / V_i(s)$. Is this a high-pass or a low-pass network? What is its transmission at very high frequencies ($s \rightarrow \infty$)? What is the corner frequency ω_0 ? For $R_1 = 10 \text{ k}\Omega$, $R_2 = 40 \text{ k}\Omega$, and $C = 0.1 \mu F$, find f_0. What is the value of $|T(j\omega_0)|$?

2. (15%) The circuit in Fig. 2 utilizes an ideal op amplifier. (a) Find I_1, I_2, I_3 and V_X. (5%) (b) If V_o is not to be lower than -13 V, find the maximum allowed value for R_L. (5%) (c) If R_L is varied in the range 100 Ω to 1 kΩ, what is the corresponding change in I_L and in V_O ? (5%)

3. (15%) The NMOS and PMOS transistors in the circuit of Fig. 3 are matched with $k_n' (W_n/L_n) = k_p' (W_p/L_p) = 1 \text{ mA/V}^2$ and $V_{tn} = -V_{tp} = 1V$. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP} and the voltage v_o for $v_I = 0V$, +2.5V, and -2.5V.

4. (20%) For the common-emitter amplifier shown in Fig. 4, let $V_{CC} = 9$ V, $R_1 = 27$ kΩ, $R_2 = 15$ kΩ, $R_E = 1.2$ kΩ, and $R_C = 2.2$ kΩ. The transistor has $\beta = 100$ and $V_A = 100V$. Calculate the dc bias current I_E. If the amplifier operates between a source for which $R_{sig} = 10$ kΩ and a load of $R_L = 2$ kΩ, replace the transistor with its hybrid-π model, and find the values of R_{in}, the voltage gain v_o/v_{sig}, and the current gain i_o/i_i.

5. (20%) The op amplifier in the circuit of Fig. 5 has an open-loop gain of 10^5 and a single-pole rolloff with $\omega_{3dB} = 10$ rad/s. (a) Sketch a Bode plot for the loop gain. (6%) (b) Find the frequency at which $|A\beta| = 1$, and find the corresponding phase margin. (6%) (c) Find the closed-loop transfer function, including its zero and poles. Sketch a pole-zero plot. (8%)

6. (15%) A BJT is specified to have $T_{J \, max} = 150$ ^{O}C and to be capable of dissipating maximum power as follows:

$$40 \text{ W at } T_C = 25 \text{ }^O\text{C}$$
$$2 \text{ W at } T_A = 25 \text{ }^O\text{C}$$

Above 25 ^{O}C, the maximum power dissipation is to be derated linearly with $\theta_{JC} = 3.12$ ^{O}C/W and $\theta_{JA} = 62.5$ ^{O}C/W. Find the following: (a) The maximum power that can be dissipated safely by this transistor when operated in free air at $T_A = 50$ ^{O}C. (5%) (b) The maximum power that can be dissipated safely by this transistor when operated at an ambient temperature of 50 ^{O}C, but with a heat sink for which $\theta_{CS} = 0.5$ ^{O}C/W and $\theta_{SA} = 4$ ^{O}C/W. Find the temperature of the case and of the heat sink. (5%) (c) The maximum power that can be dissipated safely if an infinite heat sink is used and $T_A = 50$ ^{O}C. (5%) (note: θ_{JA}, θ_{JC}, θ_{CS}, and θ_{SA} are the thermal resistances between junction and ambience, junction and transistor case, transistor case and heat sink, and heat sink and ambience, respectively.)

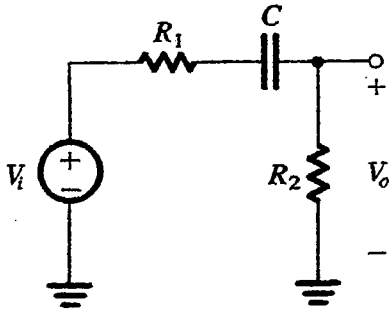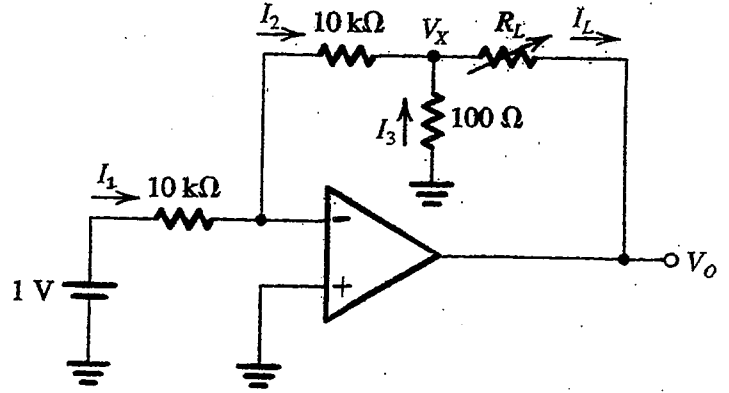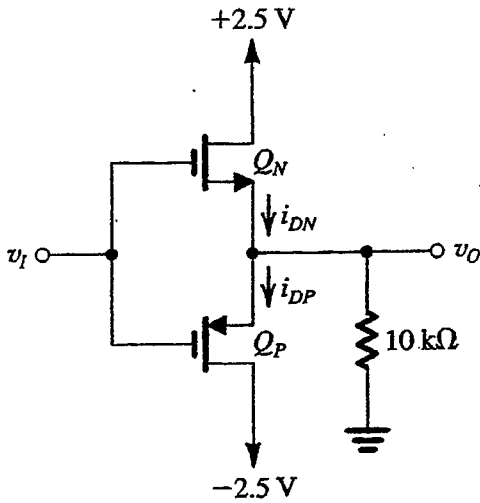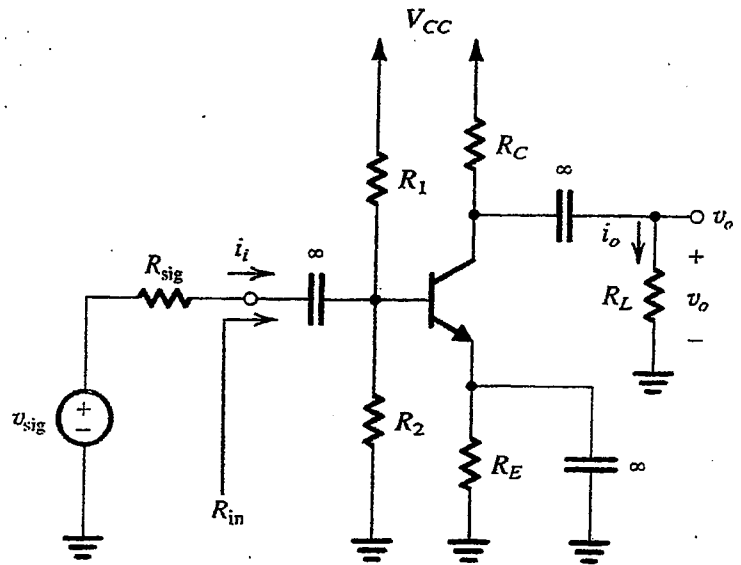# 國立中山大學100學年度碩士班招生考試試題

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Figure 1

Figure 2

Figure 3

Figure 4

Figure 5