國立中山大學100學年度碩士班招生考試試題

科目：計算機結構【電機系碩士班丙組、庚組】

[Problem 1] Briefly describe what three techniques are possible for I/O operations. (15%)

[Problem 2] (a) Describe the definition of Amdahl's law. (5%)
(b) Suppose we enhance a machine making all floating-point instructions run five times faster. If the execution time of some benchmark before the floating-point enhancement is 60 seconds, what will the speedup be if three-forth of the 60 seconds are spent executing floating-point instructions? (15 %)

[Problem 3] Given a 32-bits fast adder (named as ADD32), a 32-bits 2-to-1 Multiplexor (named as MUX32_2to1), as Figure 1, and the basic gates such as NOT, AND, OR, NAND, NOR and XOR, you are asked to design an ALU, which must match the following requirements: (in function block diagrams) (20%)

(1) Support add, sub, and slt instructions. Their operation selection bits (op_sel) are as follows:
add(00), sub(01), slt(11).
(2) Report the result status in sign, zero, overflow, and carry bits.

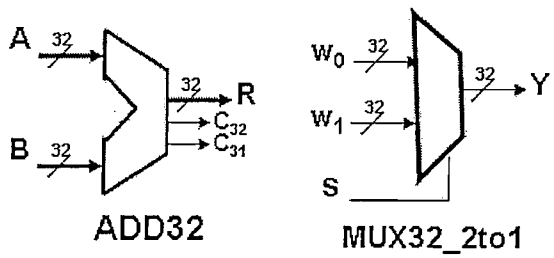

Figure 1

[Problem 4] A set associative cache has a block size of four 32-bit words and a set size of 4. The cache can accommodate a total of 4K words. The main memory size that is cacheable is 256K * 32 bits. Design the cache structure and show how the processor's addresses are interpreted. (20%)

[Problem 5] Use the following code fragment:

```
Loop:   LW      R1, 0(R2)
        ADDI    R1, R1, #1
        SW      0(R2), R1
        ADDI    R2, R2, #4
        SUB     R4, R3, R2
        BNEZ    R4, Loop
```

Assume the initial value of R3 is R2+200. Use the five-stage instruction pipeline (IF, DEC, EXE, MEM, WB) and assume all memory accesses are one cycle operation. Furthermore, branches are resolved in MEM stage.

(a) Show the timing of this instruction sequence for the five-stage instruction pipeline with normal forwarding and bypassing hardware. Assume that branch is handled by predicting it as not taken. How many cycles does this loop take to execute? (15%)
(b) Assuming the five-stage instruction pipeline with a single-cycle delayed branch and normal forwarding and bypassing hardware, schedule the instructions in the loop including the branch-delay slot. You may reorder instructions and modify the individual instruction operands, but do not undertake other loop transformations that change the number of op-code of instructions in the loop. Show a pipeline timing diagram and compute the number of cycles needed to execute the entire loop. (10%)