[Problem 1] Please use one 4-bit adder, one 2-bit adder, and a few logic gates (AND, OR, or NOT) to implement a one-digit BCD adder with one carry-in bit and one carry-out bit. Please note that the details of the adders are no need to show. (20%)

[Problem 2] In addition to the BCD code, 2-4-2-1 code listed below is also a useful coding to represent decimal digits in self complementing manner. Please design a function $F$ to check if the decimal input encoded by 2-4-2-1 code can be exactly divided by three. In other words, $F = 1$ if and only if the reminder of the division by 3 is zero. Make the truth table of this function and design the two-level NOR-NOR network with minimum number of logic gates and literals. Note that the input code words ($a$, $b$, $c$, $d$) and their complements can be used directly as fan-in in the logic circuit. (15%)

Table 1

| Decimal digit | 8-4-2-1 Code (BCD) | 2-4-2-1 Code |
|---|---|---|
| 0 | 0000 | 0000 |
| 1 | 0001 | 0001 |
| 2 | 0010 | 0010 |
| 3 | 0011 | 0011 |
| 4 | 0100 | 0100 |
| 5 | 0101 | 1011 |
| 6 | 0110 | 1100 |
| 7 | 0111 | 1101 |
| 8 | 1000 | 1110 |
| 9 | 1001 | 1111 |

[Problem 3] The sequential circuit in figure 1 has one input signal $X$ that is synchronized with the clock and one output signal $Z$.

(a) Complete the state table. (6%)

(b) It is known that this circuit is a sequence detector and is initialized to $AB = 00$ when powered up. What sequence(s) does it detect? (9%)

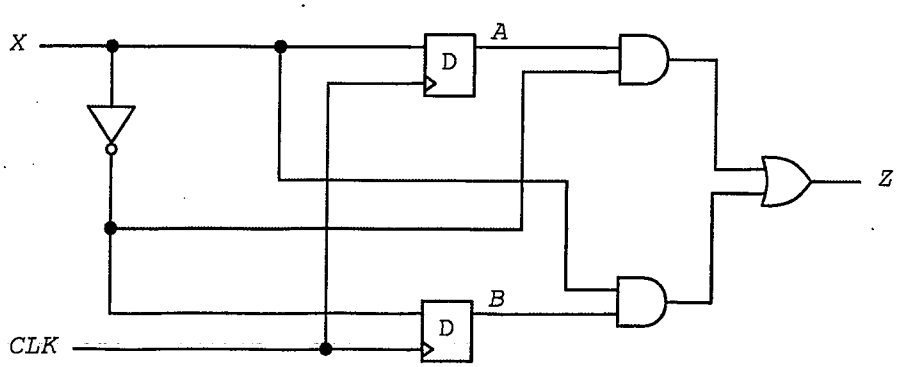


Figure 1

# 國立中山大學100學年度碩士班招生考試試題

科目：數位電路【電機系碩士班丙組選考、庚組】

[Problem 4] A Moore sequential network has one input and one output. When the input sequence 101 occurs, the output becomes 1 and remains 1 until the sequence 101 occurs again, in which case the output returns to 0. The output then remains 0 until 101 occurs a third time, and so forth. For example, the input sequence

X = 0 1 0 1 1 0 1 0 1 1 0 1 0 0 1 1

has the output

Y = 0 0 0 1 1 1 0 0 1 1 1 0 0 0 0 0

Derive the state diagram with a minimum number of states. Notice that you have to verify that the number of state in your design has been minimized. (15%)

[Problem 5] A timing chart as below is recorded on a Mealy machine with one input X, one output Z, and two JK flip-flops. Construct the state table and draw the sequential circuit. (15%)

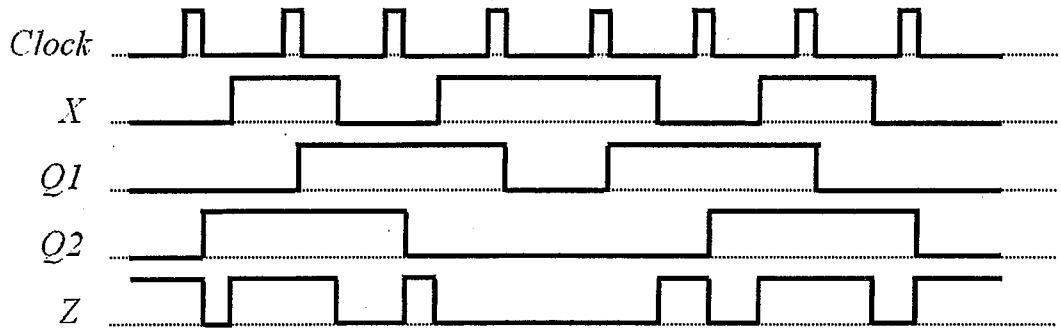


Figure 2

[Problem 6] A switching network has three inputs and two outputs, $a$ and $b$, which represent the first and second bits of a binary number ($N$) respectively. Here $N$ equals the number of inputs which are 0. For example, if $x = 1, y = 0$, and $z = 0$, then $a = 1, b = 0$. Please implement this network with two 4-to-1 multiplexers. (20%)

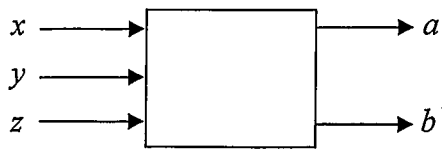


Figure 3