1. In each of the following statements, determine whether the statement is True or False. Describe your reasons to support your choices.

   (a)As the biasing current increases, the MOS transconductance increases linearly with respect to biasing current. (5%)

   (b)The dominant current in MOS devices is drift current. (5%)

   (c)When the substrate reverse bias of an NMOS device is increased, the threshold voltage will decrease. (5%)

2. Find the voltage gain of the differential amplifier circuit of Fig. P2 under the condition that I_1 = 60μA, V_t = 1V, $W_1 = W_2$ = 3.5μm, $L_1 = L_2$ = 0.35μm, $C_{ox}\mu_n$ = 150μA/V², $C_{ox}\mu_p$ = 75μA/V², V_A (Both NMOS and PMOS) = 20V. (10%)

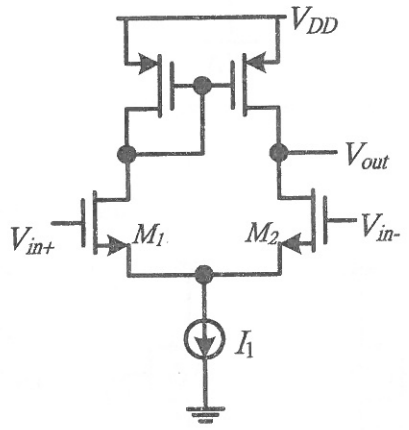


Fig. P2

3. Consider a feedback amplifier for which the open-loop transfer function $A(s)$ is given by

$$A(s) = \left(\frac{10}{1 + s/10^5}\right)^3$$

   (a)Draw the Bode plot. (10%)

   (b)Let the feedback factor β be a constant independent of frequency. Find the frequency ω_{180} at which the phase shift is 180°. (5%)

   (c)Show that the feedback amplifier will be stable if the feedback factor is less than a critical value β_{cr} and find the value of β_{cr}. (10%)

4. The circuit of Fig. P4 is fabricated with the following process parameters: $C_{ox}\mu_n$ = 100 μA/V², $C_{ox}\mu_p$ = 50 μA/V², and V_{tn} = $|V_{tp}|$ =0.5V. Assume that $5(W/L)_{QREF}$= $4(W/L)_{Q1}$ = $3(W/L)_{Q2}$ = $2(W/L)_{Q3}$ = $1.5(W/L)_{Q4}$, $2(W/L)_{A1}$ = $(W/L)_{A2}$ =20, L = 2 μm for Q_{A1} and Q_{A2}, λ=0 for Q_{REF} and Q_1 ~ Q_4, V'_A= 10 V/μm for Q_{A1}, and V'_A= 5 V/μm for Q_{A2}.

(a) Calculate I_1 and I_2. (5%)

(b) In case both Q_{A1} and Q_{A2} are biased at saturation region, please find the voltage gains v_{o1}/v_{i1} and v_{o2}/v_{i2}. (10%)

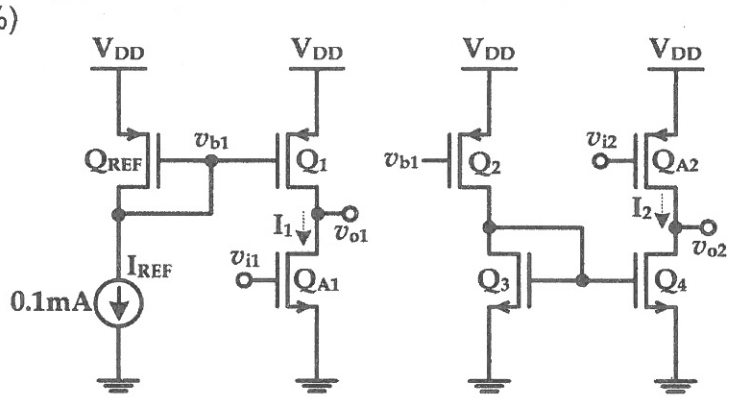


Fig. P4

5. (a) Please explain the miller theorem. (5%)

(b) Please determine the input and output poles of the circuits shown in Fig. P5. Assume that the parasitic capacitances of a MOS transistor are C_{GS}, C_{GD}, and C_{DB}. (10%)

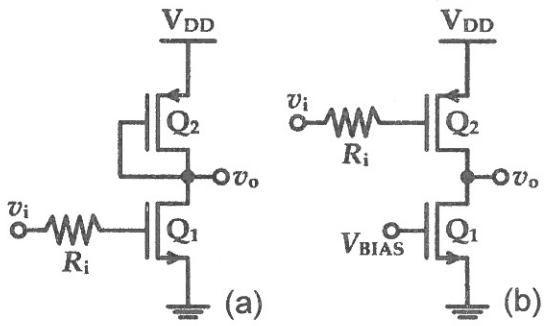


Fig. P5

6. (a) A CMOS inverter is designated using the following parameters: V_{DD} = 1.8 V, V_{tn} = 0.5 V, $|V_{tp}|$ = 0.5V, $C_{ox}\mu_n$ = 300 μA/V², $C_{ox}\mu_p$ = 75 μA/V², $(W/L)_{PMOS}$ = 1.08 μm/0.18 μm, $(W/L)_{NMOS}$ = 0.27 μm/0.18 μm, and ignore the channel length modulation. Please calculate the noise margins. (10%)

(b) Assume that an equivalent capacitance C_L exists between the output node of the CMOS inverter and ground. In case the inverter is switched at a frequency of *f* Hz with a supply voltage of V_{DD}, please derive the dynamic power dissipation of the inverter. (5%)

(c) If two CMOS inverters are designated with the characteristics shown in Fig. 6P(a), please sketch the overall voltage-transfer characteristic (VTC) for the circuit configurations shown in Fig. 6P(b). (5%)

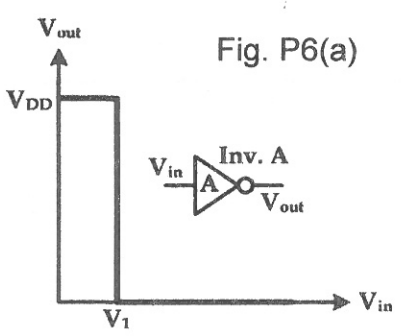
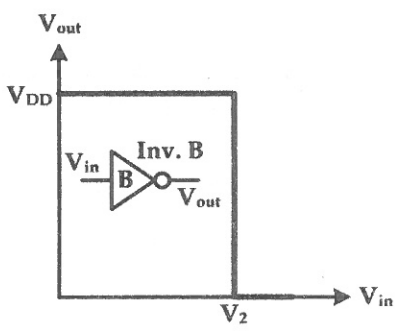


Fig. P6(a)



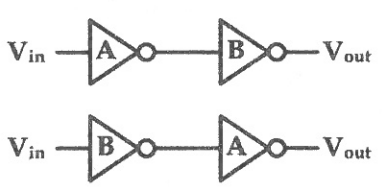


Fig. P6(b)