國立嘉義大學 104 學年度

電機工程學系碩士班招生考試試題

科目：電子學 (可使用工程計算機)

1. If V_1=5 cos2t mV and V_2=2t mV, find V_o in the op amp circuit as shown in Fig. 1 below. Assume that the voltage across the capacitor is initially zero. (15 %)

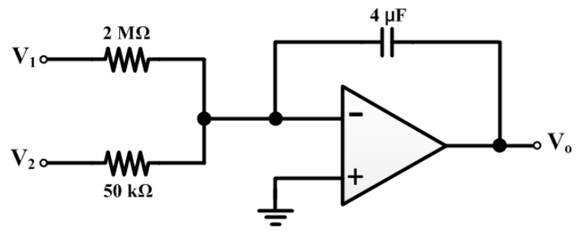

Fig. 1

2. If V_1=7 V and V_2=3.1 V, find V_o in the op amp circuit as shown in Fig. 2 below. (15 %)

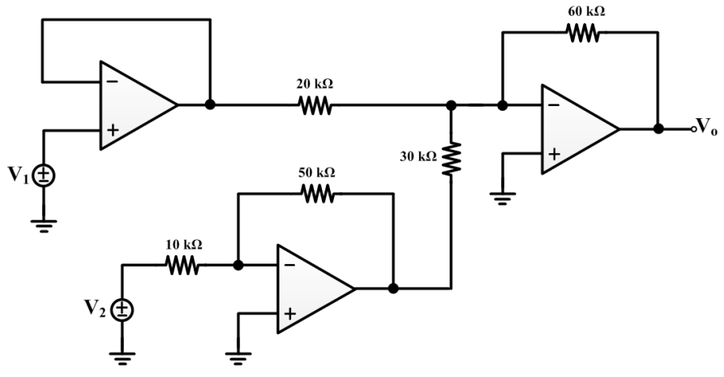

Fig. 2

3. The transistor in the circuit of Fig. 3 has a very high β. Assume V_{BE} = 0.7 V. Find

   (a) For V_B = +2 V, find V_E and V_C. (Each answer takes 8%)

   (b) For V_B = +1 V, find V_E and V_C. (Each answer takes 8%)

   (c) For V_B = 0 V, find V_E and V_C. (Each answer takes 8%)

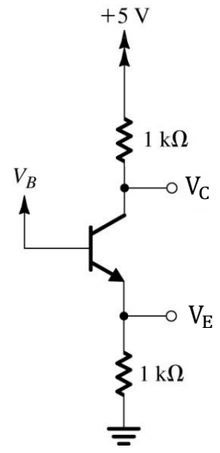

Fig. 3

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4. Consider the basic BJT current mirror of Fig. 4, when Q_1 and Q_2 are matched devices having $I_S = 10^{-15}$ A.

(a) If β of the transistor is 20, what is the current gain "I_O / I_{REF}"? Neglect the Early effect. (8%)

(b) If I_{REF} = 2 mA, and the Early voltage is 90 V. Neglecting the effect of finite β, V_O changing from 1 V to 10 V, find the change in "ΔI_O". (8%)

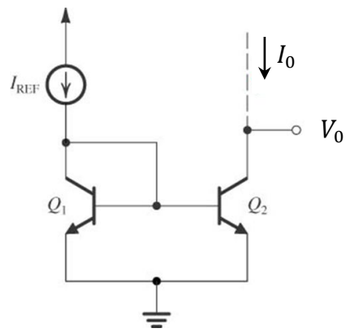

Fig. 4

5. In the circuit of Fig. 5, the NMOS transistor has $|V_t|$ = 0.9 V and V_A = 50 V and operates with V_D = 2 V. What is the voltage gain "v_o/v_i"? (12 %)

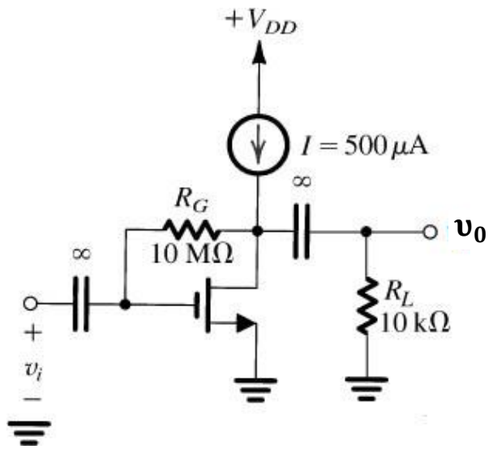

Fig. 5

6. The NMOS transistors in the circuit of Fig. 6 have Vt = 1 V, $\mu_n C_{ox}$ = 120 μA/V^2, λ = 0, and $L_1 = L_2$ = 1 μm. Find required values to obtain the voltage and current values indicated.

(a) Find the required value of gate width "W_1" for Q_1. (6%)

(b) Find the required value of gate width "W_2" for Q_2. (6%)

(c) Find the value of "R". (6%)

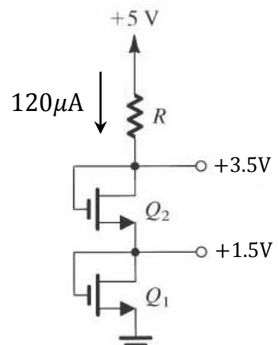

Fig. 6