

國立臺灣海洋大學 101 學年度研究所碩士班暨碩士在職專班入學考試試題

考試科目：電子學（含半導體元件物理）

系所名稱：電機工程學系碩士班固態電子組

*可使用計算器

1. 答案以橫式由左至右書寫。2. 請依題號順序作答。

PART I : (共 50 分)

1. In the circuit of Fig. 1, assume the turn on voltage of the diode is $V_D = 0.7$ V, draw the output voltage v_o versus time diagram. (6%)

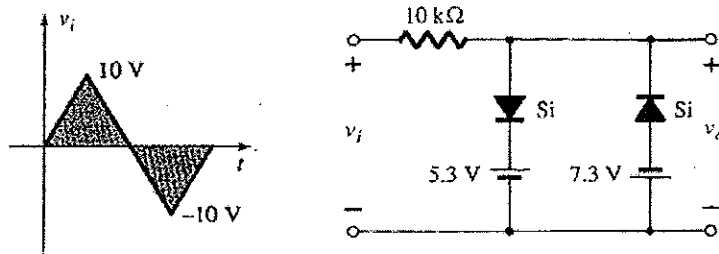


Fig. 1

2. Determine the gain $A_v = \frac{v_o}{v_i}$ for the ideal op-amp circuits shown in Fig. 2(a) and 2(b). (8%)

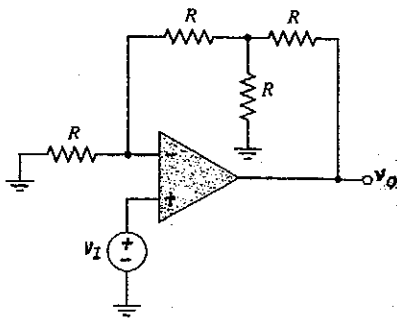


Fig. 2(a)

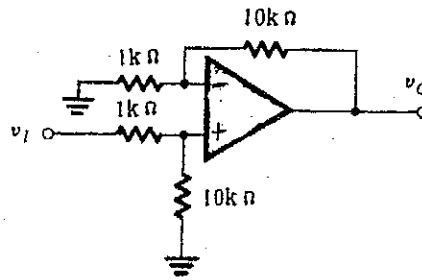


Fig. 2(b)

3. For the common-emitter amplifier of Fig. 3, let

$I_C = 1\text{mA}$, $\beta = 100$, $V_A = 100\text{V}$, $R_C = 5\text{k}\Omega$, $R_S = 5\text{k}\Omega$, thermal voltage $V_T = 25\text{mV}$. Find R_i , A_v , and R_o . (12%)

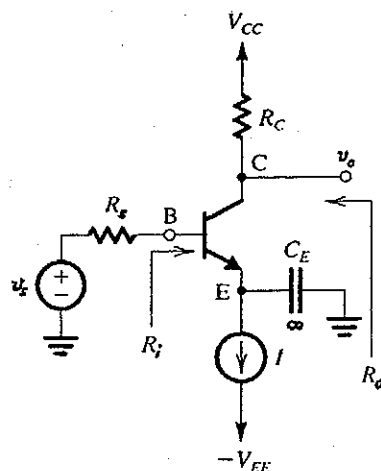


Fig. 3

4. An NMOS transistor with $\lambda = 0$, threshold voltage $V_{th} = 1.0V$ has a drain current $i_D = 0.8mA$ when $v_{GS} = 3V$ and $v_{DS} = 4.5V$. Calculate the drain current when:
 (a) $v_{GS} = 2V$ and $v_{DS} = 4.5V$; and (b) $v_{GS} = 3V$ and $v_{DS} = 1V$. (6%)
5. Consider the CMOS common-source amplifier in Fig. 4, assume Q2 and Q3 are matched, and $V_{DD} = 10V, V_m = |V_{ip}| = 1V, |V_{A1}| = |V_{A2}| = 50V, \mu_n C_{ox} = 2.5\mu_p C_{ox} = 50\mu A/V^2$. Find I_{REF} and $(W/L)_1$, to obtain a voltage gain of $-100 V/V$ and an output impedance of $1 M\Omega$. (8%)

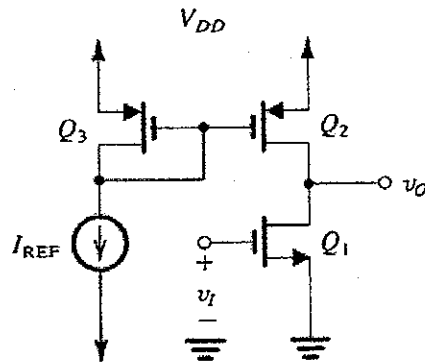


Fig. 4

6. For the signal and circuit of Fig. 5 determine the maximum frequency that may be used to prevent distortion. The slew rate of op-amp is $SR = 0.5 V/\mu s$. (4%)

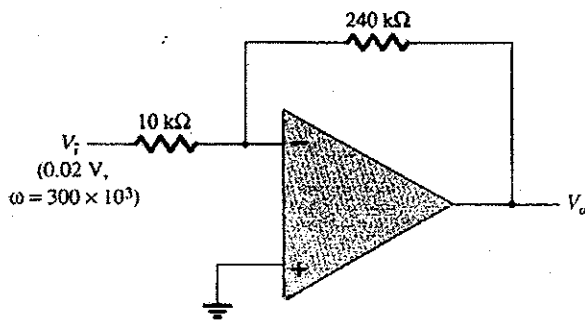


Fig. 5

7. A series-shunt feedback amplifier employs a basic amplifier with input and output resistances each of $1k\Omega$ and gain $A=1000 V/V$. The feedback factor $\beta=0.1 V/V$. Find the gain A_f , the input resistance R_{if} , and the output resistance R_{of} of the closed-loop amplifier. (6%)

PART II : (共 50 分)

1. 以基本的半導體元件物理的觀念及手上僅有的三用電錶為工具，以三用電錶所量測到的數據，皆以”高”或”低”的比較值來描述，回答下列問題。
- (1) 在實驗桌上遺留一顆未知的三端元件，很可能是BJT, JFET及MOSFET其中之一。請詳細說明以三用電錶分別判斷BJT, JFET及MOSFET這三個元件的方法(用歐姆檔、電壓檔還是電流檔，高數值還是低數值)(9%)及所代表的半導體元件物理的觀念(高摻雜、低摻雜還是絕緣體，pn接面順向或逆向偏壓等)(9%)，並決定EBC及SGD的腳位(6%)。

- (2) 承(1)題，如果是BJT，如何決定是 pnp 還是 npn 型？(3%)
 (3) 承(1)題，如果是FET，如何決定是 JFET 還是 MOSFET? (3%)

2.圖一為電阻式負載 nMOS 反向器，回答下列問題：

- (1) 在同一張圖中畫出電晶體的輸出特性曲線及負載線。(2%)
 (2) 畫出 V_o/V_i 轉移曲線。(3%)

3.圖二為增強型電晶體主動式負載 nMOS 反向器，回答下列問題：

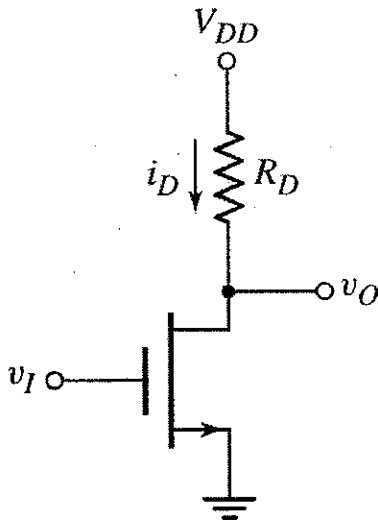
- (1) 在同一張圖中畫出電晶體的輸出特性曲線及負載線。(2%)
 (2) 畫出 V_o/V_i 轉移曲線。(3%)

4.圖三為空乏型電晶體主動式負載 nMOS 反向器，回答下列問題：

- (1) 在同一張圖中畫出電晶體的輸出特性曲線及負載線。(2%)
 (2) 畫出 V_o/V_i 轉移曲線。(3%)

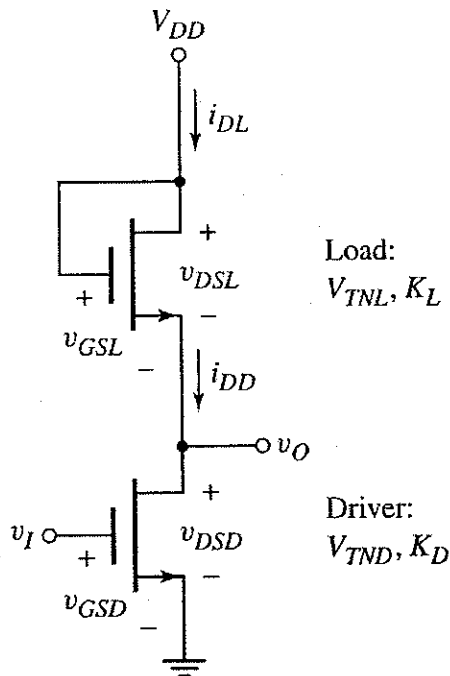
5.圖四為 CMOS 反向器，回答下列問題：

- (1) 在同一張圖中畫出兩個電晶體的輸出特性曲線。(2%)
 (2) 畫出 V_o/V_i 轉移曲線。(3%)

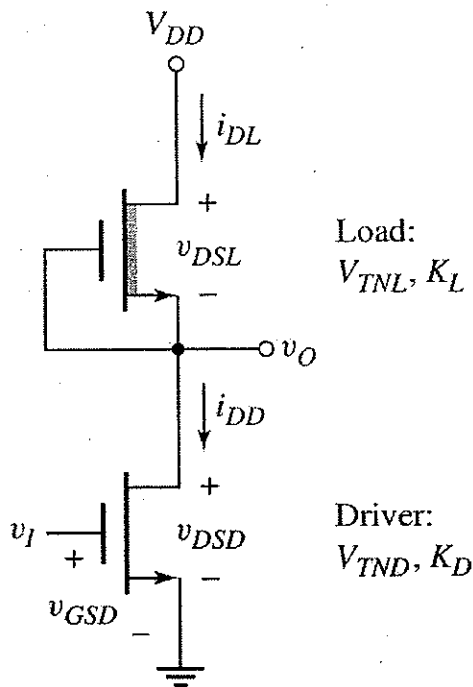


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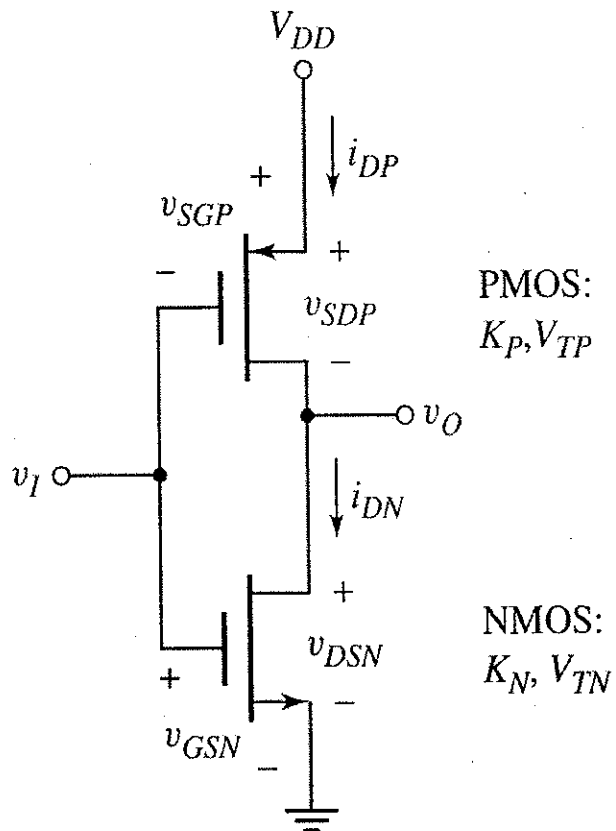
圖一



圖二



圖三



圖四