國立成功大學 104 學年度碩士班招生考試試題

系所組別：電機資訊學院-微電、奈米聯招

考試科目：固態電子元件

考試日期：0211，節次：2

※考生請注意：本試題可使用計算機。請於答案卷(卡)作答，於本試題紙上作答者，不予計分。

Useful constants:

electron charge = 1.6×10^{-19} C

kT = 0.0259 eV

Permittivity of free space $\varepsilon_0 = 8.85\times10^{-14}$ F/cm

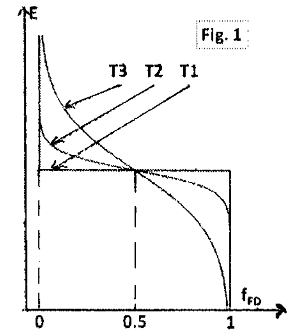
Silicon (Si):

- Electron affinity χ = 4.01 V
- Bandgap energy = 1.12 eV
- Dielectric constant = 11.7
- $N_c = 2.8\times10^{19}$ cm^{-3}
- $N_v = 1.04\times10^{19}$ cm^{-3}
- $n_i = 1.5\times10^{10}$ cm^{-3}

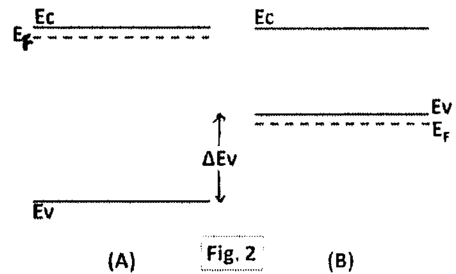
Oxide (SiO_2)

- dielectric constant = 3.9

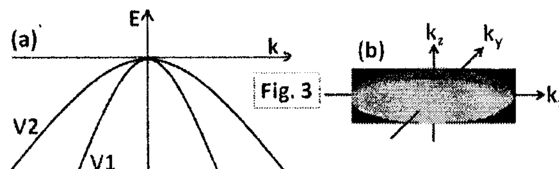
1. Fig. 1 shows the Fermi-Dirac distribution f_{FD} as a function of energy E at different temperature. Which curve display the distribution at the highest temperature (3%)? Please explain why the distribution is different in energy at different temperature (5%)? How to define Fermi level at absolute zero degree (3%)? How to define Fermi level at room temperature (3%)?



2. Fig. 2 shows the conduction Ec and valence Ev band edges of two isolated semiconductors A and B. The dashed lines are their Fermi levels. Which one is degenerately doped (4%)? Please draw the band diagram with a clear indication of ΔEv when they are attached at thermal equilibrium (8%).



3. Fig. 3(a) plots the valence band structure of a semiconductor for a given direction k. Please explain which band (V1 and V2) exhibits the lighter effective mass in k direction (4%). Considering a constant energy surface of the conduction band minimum in k-space as shown in Fig. 3(b). If electrons can occupy this valley, at which direction electrons exhibit the heaviest effective mass (4%)?



4. Considering a degenerately-doped tunnel diode ($p^{++}n^{++}$ junction), Fig. 4 shows the current-voltage characteristics and corresponding band diagrams at different bias V conditions. Please draw the missing band diagram at V = 0 V for (a, 8%) and reverse bias for (e, 8%). Please clearly indicate the Fermi level E_F, conduction E_C and valence E_V edges.

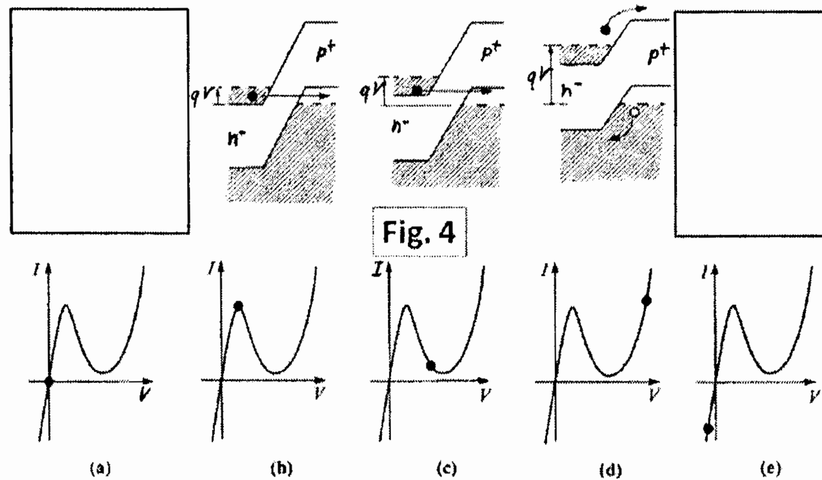


Fig. 4

5. Consider an MOS capacitor with aluminum gate, gate oxide of t_{ox} = 2.2 nm, and p-type silicon substrate of $N_a = 10^{16}$ cm^{-3}. Assume low frequency operation. When the substrate is biased in the strong inversion region, (a) calculate space charge (depletion region) width (10%) and (b) calculate (estimate) the capacitance value (in F/cm^2) of the MOS capacitor. (10%)

6. For an npn bipolar transistor with base width x_{B0} = 0.65 μm, $N_E = 8 \times 10^{17}$ cm^{-3}, $N_B = 2 \times 10^{16}$ cm^{-3}, and $N_C = 5 \times 10^{15}$ cm^{-3}. Neglect the B-E space charge width. Find the punch-through voltage. (10%)(Hint: think about the depletion region of the pn junction.)

7. Consider an MOS device with p-type silicon substrate with doping $N_a = 2 \times 10^{16}$ cm^{-3}. For an n^+-polysilicon gate, find the work function difference (ϕ_{ms}). (10%)

8. Ignore C_μ, C_s, r_μ, C_{je}, and r_o in the simplified hybrid-pi equivalent circuit. Given r_π = 2.6 kΩ and C_π = 4 pF, calculate the frequency at which the small-signal current gain decreases to $1/\sqrt{2}$ of its low-frequency value as shown in Fig. 5. (f = ? MHz) (10%)

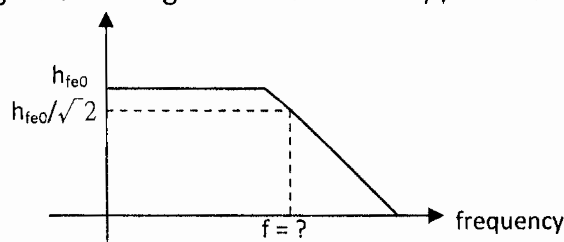


Fig. 5