國立臺北大學104學年度碩士班一般入學考試試題

系（所）組別：電機工程學系甲組(晶片設計組)

科　　目：電子學B

☐可 ☑不可使用計算機

每題10分

1. The open-loop amplifier gain A_0 is not infinite, derive the transfer function V_{out}/V_{in} of the circuit shown in Fig. 1 considering A_0.
2. (a) Derive the transfer function $V_{out}(s)/V_{in}(s)$ of the circuit shown in Fig. 2, (b) derive its pole frequency.
3. For the differential amplifier shown in Fig. 3, (a) Define its common-mode rejection ratio (CMRR)? (b) What is the purpose to design a high CMRR?
4. For the circuit shown in Fig. 4, (a) Which mode is Q1 operated? (b) Explain why?
5. (a) Draw the small-signal model of the circuit shown in Fig. 5, (b) Derive its output impedance, including the Early effect.
6. For the circuit shown in Fig. 6, (a) How do we choose bias voltage V_b? (b) Why should R_E be much bigger than input impedance $1/g_m$ of Q_1?
7. The feedback system shown in Fig. 7 has an open-loop amplifier $A_1(s)=A_0/(1+s/\omega_0)$, where $s=j\omega$ and $\omega=2\pi f$, f is the frequency, A_0 and ω_0 are the dc gain and pole frequency of the open-loop amplifier, respectively. Find the close-loop gain and close-loop bandwidth of Y(s)/X(s)?
8. Draw the small-signal mode of the circuit shown in Fig. 8 and derive its dc gain, ignoring body effect but including channel length modulation?
9. For the circuit shown in Fig. 9, C_{GS}, C_{GD}, C_{DB} and C_{SB} are parasitic capacitances of M1, derive the poles at nodes X and Y?
10. Derive the open-loop gain and feedback gain of the close loop system shown in Fig. 10?

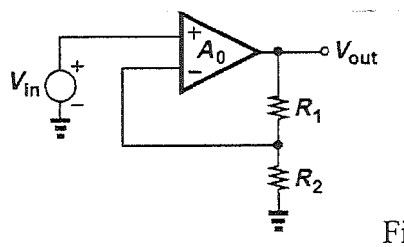

Fig. 1

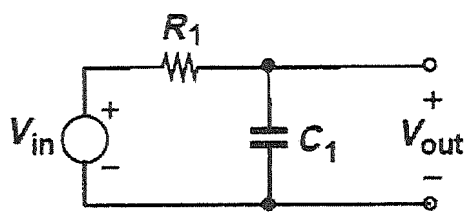

Fig. 2

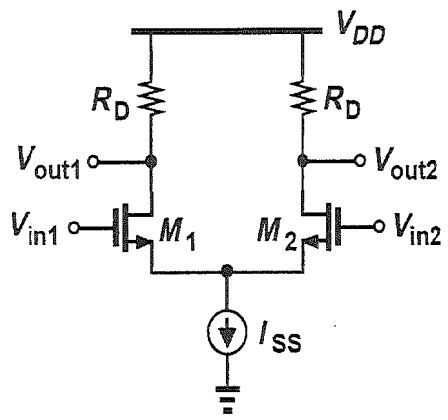

Fig. 3

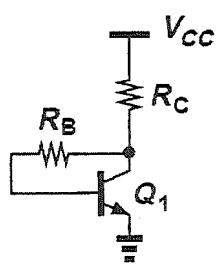

Fig. 4

試題隨卷繳交

接背面

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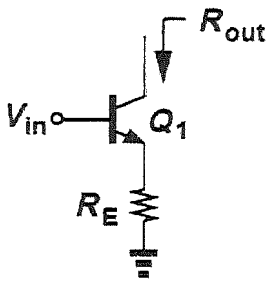

Fig. 5

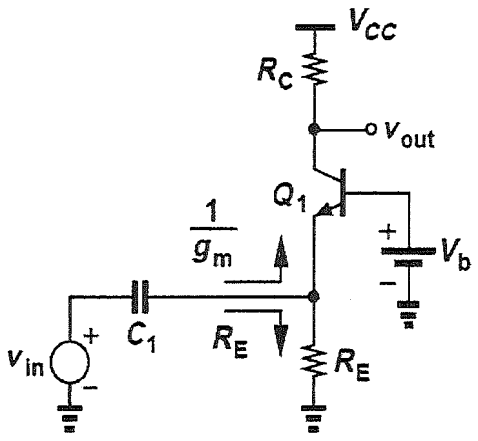

Fig. 6

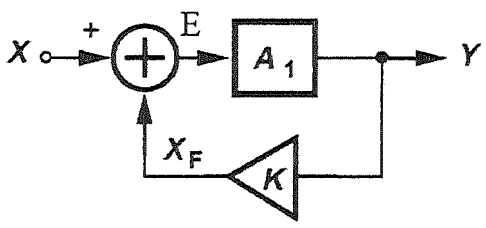

Fig. 7

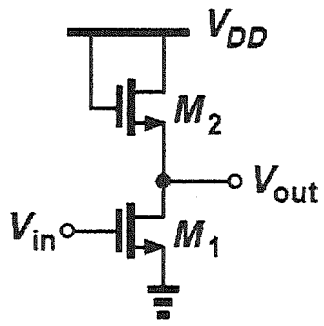

Fig. 8

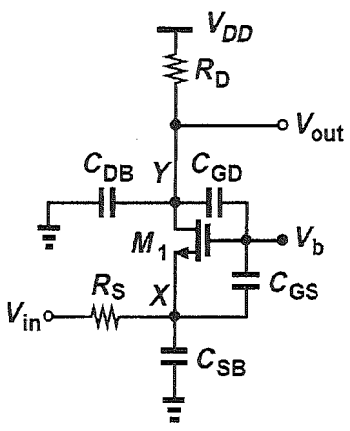

Fig. 9

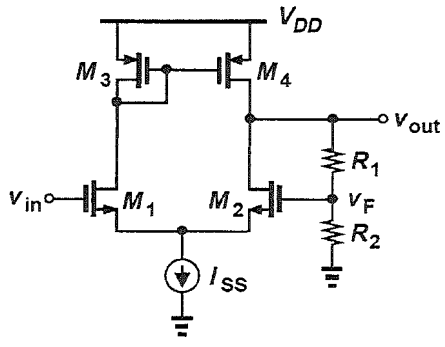

Fig. 10

試題隨卷繳交