1. Fill the blanks with either 0 or ∞. **[12pts**, each blank 2pts]
   (a) An ideal transimpedance amplifier has its input resistance, R_{in} = _____, and output resistance, R_{out} = _____.
   (b) An ideal operational amplifier would provide _____ voltage gain, _____ input impedance, _____ output impedance, and _____ bandwidth.

2. For a saturation MOSFET, how its transconductance, g_m, changes for the following conditions? [**8 pts**, each blank 2pts]
   (a) W/L is doubled but I_D remains constant. g_m will _____.
   (b) $V_{GS} - V_{TH}$ is doubled but I_D remains constant. g_m will _____.
   (c) I_D is doubled but W/L remains constant. g_m will _____.
   (d) I_D is doubled but $V_{GS} - V_{TH}$ remains constant. g_m will _____.

3. In Fig. 1, assume the diodes are ideal. Plot the input/output characteristic. [**5 pts**]

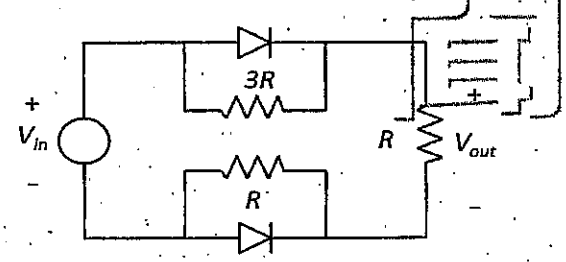

Fig. 1

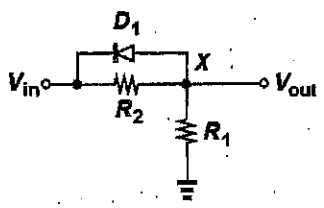

Fig.2

4. In Fig. 2, $R_1 = 2\,R_2$. Assume D_1 behaves as an ideal switch with a turn on voltage of 0.6V. Plot the input/output characteristic. [**5 pts**]

5. In Fig. 3, (a) what is the logic function of the circuit? [**5 pts**] (b) Assume $\mu_n = \mu_p$ and equal channel length of MOS's. And the channel width of M_3 is W. Determine the widths of the other MOS's to make the output of the circuit have equal rise and fall times. [**5 pts**]

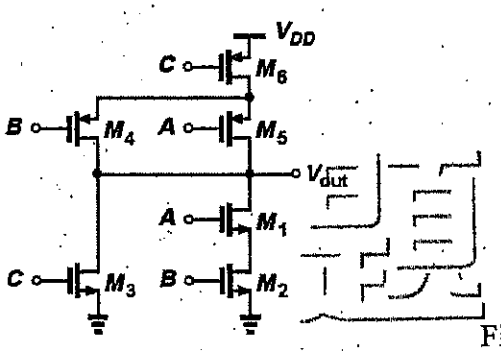

Fig. 3

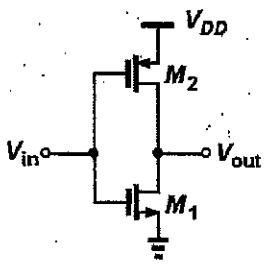

Fig. 4

6. Fig. 4 is a CMOS inverter. (a) Plot its voltage transfer characteristic. [**5 pts**] (b) Label the five different operation status of M_1 and M_2 in the plot. [**5 pts**]

7. Assume the op amps in Fig. 5 are ideal. (a) Determine Z_{in}. **[5 pts]** (b)What type of component the circuit simulated? **[5 pts]**

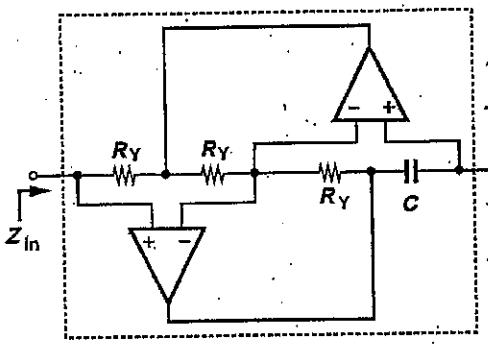

Fig. 5

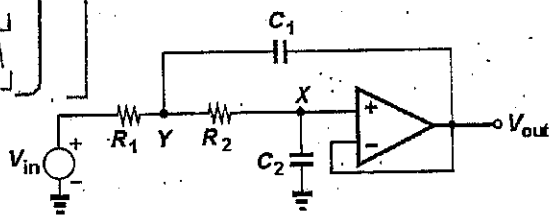

Fig. 6

8. Assume the op amp in Fig. 6 is ideal. (a) Derive the transfer function, $V_{out}/V_{in}(s)$. **[5 pts]** (b) What type of filter the circuit realized? **[5 pts]**

9. Assume the op amp in Fig. 7 is ideal. (a) Derive $H(s) = V_{out}/V_{in}(s)$. **[5 pts]** (b) Plot the frequency response of $H(\omega)$ for $R_1C_1 < R_2C_2$. **[5 pts]**

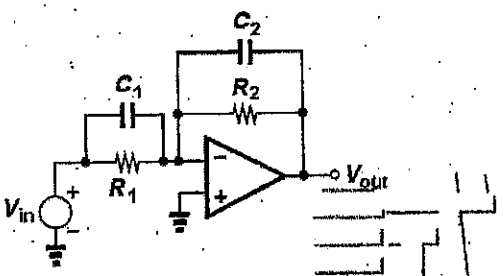

Fig. 7

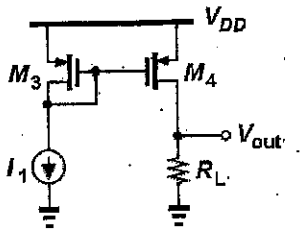

Fig. 8

10. Determine the small-signal gain v_{out}/i_1 of the circuit in Fig. 8 if $(W/L)_3 = N\,(W/L)_4$. **[5 pts]**

11. Determine the closed-loop gain of the circuit in Fig. 9 if $A_0 = \infty$. **[5 pts]**

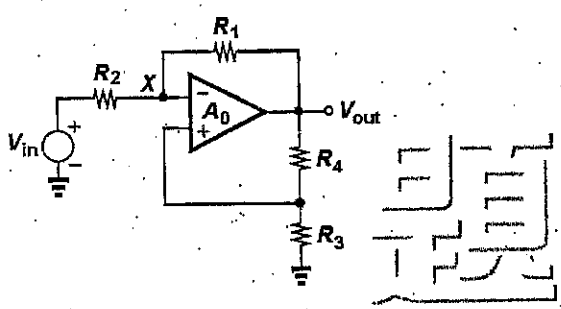

Fig. 9

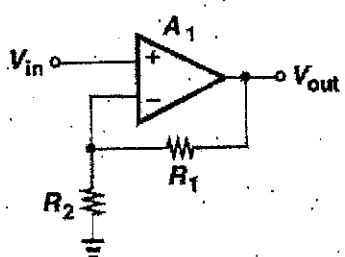

Fig. 10

12. The circuit in Fig. 10 is designed for a nominal gain of 10, i.e., $1 + R_1/R_2 = 10$. Determine the minimum value of A_1 for a gain error of 1%. Assume $(1 + x)^{-1} \approx 1 - x$. **[10 pts]**