國立臺灣師範大學 104 學年度碩士班招生考試試題

科目:計算機系統

適用系所:資訊工程學系

注意:1.本試題共 3 頁,請依序在答案卷上作答,並標明題號,不必抄題。2.答案必須寫在指定作答區內,否則不予計分。

- 1. (4 分) Convert the following unsigned 8-bit binary numbers to decimal numbers:
 - (a) (2分) 01110101
 - (b) (2分) 11100000
- 2. (6 分) Consider a CPU with clock cycle time 0.5 nanosecond (or 0.5 ns). Suppose the CPU executes a program with 1000 instructions. The average CPI (clock cycles per instruction) is 2.0 for the program.
 - (a) (3 分) Find the clock rate of the CPU (in gigahertz, or GHz).
 - (b) (3 分) Find the CPU time for executing the program (in ns).
- 3. (10 分) Consider a MIPS processor with separate instruction and data memories. Suppose the following code sequence is executed on the processor.

LW R4,24(R2); $R4 \leftarrow MEM[R2+24]$ R5,R1,R4; **SUB** R5 ← R1-R4 LW R12,32(R2); $R12 \leftarrow MEM[R2+32]$ **ADD** R8,R12,R4; $R8 \leftarrow R12+R4$ ADD R10,R2,R8; $R10 \leftarrow R2+R8$ LW R6,8(R1); $R6 \leftarrow MEM[R1+8]$ LW R11,16(R1); $R11 \leftarrow MEM[R1+16]$ **SUB** R9, R11, R6 R9 ← R11-R6

- (a) (2 分) Determine the number of accesses to the instruction memory,
- (b) (2 分) Determine the number of accesses to the data memory.
- (c) (3分) Suppose there is only one miss in the instruction memory for the code sequence. Compute the miss rate of the instruction memory.
- (d) (3 分) Suppose there are two misses in the data memory for the code sequence. Compute the miss rate of the data memory.

國立臺灣師範大學104學年度碩士班招生考試試題

- 4. (20 分) Consider a five-stage (IF, ID, EX, MEM and WB) MIPS pipeline processor with hazard detection and data forwarding units. Assume the processor includes separate instruction and data memories so that the structural hazard for memory references can be avoided.
 - (a) (8 分) Suppose the following code sequence is executed on the processor. Identify all the data hazards which can be solved by forwarding.

ADD R5, R7, R12; R5 \leftarrow R7+R12 ADD R4, R5, R6; R4 \leftarrow R5+R6

LW R8,12(R4); R8 \leftarrow MEM[12+R4]

(b) (8 分) Repeat part (a) for the following code sequence.

LW R9, 20(R7); R9 \leftarrow MEM[R7+20]

ADD R1, R9, R5; R1 \leftarrow R9+R5

SW R1, 12(R6); $MEM[R6+12] \leftarrow R1$

(c) (4 分) Suppose the following code sequence is executed on the processor. Determine the total number of clocks needed to execute the code sequence.

ADD R6, R2, R3; R6 \leftarrow R2+R3 SUB R8, R5, R6; R8 \leftarrow R5-R6

- 5. $(10 \, \triangle)$ Briefly explain the following terms.
 - (a) (4 分) Program Counter.
 - (b) (3分) Control Hazard.
 - (c) (3 分) Direct Mapped Cache.
- 6. (16 分) Please answer following questions about **Memory-Management**:
 - (a) Explain the difference between internal and external fragmentation. (6 分)
 - (b) What is **dynamic loading**? Please include its advantage. (4 %)
 - (c) Address binding of instructions and data to memory address can happen at three stages. Please name the three stages. $(3 \frac{1}{12})$
 - (d) Name the three types of page table structure. (3 分)

國立臺灣師範大學 104 學年度碩士班招生考試試題

7. (10 分) For the processes shown in the table below. Assume the process arrived at the same time but in the order as they numbered.

Process	Burst (ms)
P1	10
P2	29
Р3	3
P4	7
P5	12

Please draw the **Gantt Chart** and computer the **average waiting time** using time quantum = 10 *ms* for:

- (a) Shortest-Job-First (SJF) (2分)
- (b) First-Come, First Served (FCFS) (2分)
- (c) Round-Robin (RR) (6分)
- 8. (16 分) Please answer following questions about Synchronization and Deadlock:
 - (a) Explain why **spinlocks** are not appropriate for single-processor systems yet are often used in multiprocessor systems? (4 分)
 - (b) Explain what is **race condition**? Please give an example. (4 %)
 - (c) Explain what is deadlock? (4 分)
 - (d) Name the four conditions that prevent deadlock. (4 分)
- 9. (8分) Given the following page reference sequence, please use the LRU strategy to cache and replace pages. Suppose that we have 3 available frames, each of which could cache one page. Note that the frames are initially empty.

12737084040434365026120

- (a) Show the cached pages in the frames in each step of the page reference sequence. (4 %)

