國立高雄大學 104 學年度研究所碩士班招生考試試題

科目:計算機結構與作業系統　系所：資訊工程學系　　是否使用計算機：否
考試時間：100 分鐘　　本科原始成績：100 分

I. [20%] 單選題 (每題 2 分，共 10 題)

1. Suppose we have a processor with a base CPI of 1.0, assuming all references hit in the primary cache, and a clock rate of 4 GHz. Assume a main memory access time of 100 ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 1%. How many cycles will the new CPI be if we add a secondary cache that has a 5 ns access time for either a hit or a miss and is large enough to reduce the miss rate to main memory to 0.4%?
   (A) 1.2
   (B) 2.6
   (C) 2.8
   (D) 6.5
2. Given an IEEE 754 single precision binary representation 00111111110000000000000000000000. What decimal number is represented by the float?
   (A) 0.5
   (B) 0.75
   (C) 1.5
   (D) 7.5
3. Which statement is not true?
   (A) Branch Prediction Buffer can reduce control hazard.
   (B) Forwarding can reduce data hazard
   (C) Memory interleaving is a technique for reducing memory access time through increased bandwidth utilization of the data bus
   (D) Compulsory misses occur when the cache cannot contain all the blocks needed during execution of a program
4. Assume that individual stages of the datapath have the following latencies:

IF	ID	EX	MEM	WB
250ps	350ps	150ps	300ps	200ps

   What is the total latency of an LW instruction in a pipelined and non-pipelined processor?
   (A) 1750ps, 1250ps
   (B) 1750ps, 1050ps
   (C) 1250ps, 1250ps
   (D) 1750ps, 1050ps
5. Which statement is true?
   (A) For floating-point numbers, x, y, and z, $(x+y)+z=x+(y+z)$.
   (B) The conflict misses may occur in a fully-associative cache.
   (C) For a five-stage MIPS architecture, Translation-Lookaside Buffer should be used in IF and MEM stages.
   (D) The write-through mechanism is more suitable for virtual memory systems than the write-back mechanism.

6. A microkernel is a kernel
   (A) compiled to produce the smallest size possible when stored to disk
   (B) compressed before loading in order to reduce its resident memory size
   (C) containing many optimized components to reduce resident memory size
   (D) stripped of all nonessential components
7. Which scheduler is invoked very infrequently and controls the degree of multi-programming?
   (A) CPU scheduler
   (B) short-term scheduler
   (C) medium-term scheduler
   (D) long-term scheduler
8. Which management of OS manages the space of a flash-memory drive?
   (A) memory management
   (B) process management
   (C) storage management
   (D) database management
9. Which kind of page table structure is common for address spaces larger than 32 bits?
   (A) single-level paging (B) two-level paging (C) hashed paging (D) inverted paging
10. Consider demand paging with the following page reference string:
    5,4,3,8,2,3,1,2,5,6,8, 8,3,2,1,0,5,2,4,6. The minimum number of page faults that would occur is
    (A) 6 (B) 7 (C) 8 (D) 9

II. [20%] 填充題：填入適當的**中、英文**術語 (每題 2 分，共 10 題)

1. ____1____ switches threads only on costly stalls, such as a leve-2 cache miss.
2. ____2____ is the situation where two different processors can have two different values for the same location.
3. ____3____ is caused by the first access to a block that has never been in the cache.
4. ____4____ is a structure that holds the destination program counters for branch instructions.
5. ____5____ is the principle stating that if a data location is referenced, data locations with nearby addresses will tend to be referenced soon.
6. ____6____ is the requirement for solution to critical-section problem when a process is executing in its critical section, then no other processes can be executing in their critical sections.
7. ____7____ is the mechanism that brings a page into memory by a pager only when it is needed.
8. ____8____ is a private network connecting servers and storage units.
9. The section of a process containing temporary data such as function parameters, return addresses, and local variables is called ____9____.
10. As a process runs out of its time quantum, it will enter ____10____ state.

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III. [60%] 問答題 (每題 10 分，共 6 題)

1. The five stages of MIPS pipeline are IF (instruction fetch), ID (Instruction decode and register read), EXE (Execute operation or calculate address), MEM (Access memory operand), and WB (Write result back to register). Given the following code：

   ```
   add   $5, $2, $1
   lw    $3, 4($5)
   lw    $2, 0($2)
   or    $3, $5, $3
   sw    $3, 0($5)
   ```

   Suppose the data hazards must be resolved by “stalling” the dependent instructions until the needed operand is written back to the register file. We assume that when the needed operand is written back to the register file, the dependent instruction can read the needed operand from the register file in the same clock cycle. How many NOPs and at what places that you add to make the code segment execute correctly? How many cycles do these instructions execute? You must show how to get the answer.

2. Assume that a two-way set-associative cache of 1K blocks, 1-word block size, and a 32-bit address. How many total bits are required for the cache (including valid bits)? You must show how to get the answer.

3. Consider a computer running a program that requires 300s, with 100s spent executing FP instructions, 75s executed Load/Store instructions, and 40s spent executing branch instructions. What will the speedup be if the times for FP and branch instructions are reduced by 30% and 50%, respectively? You must show how to get the answer.

4. *write*() is a system call and *fwrite*() is a standard C library call.
   (a). Discuss their differences in the runtime environment.
   (b). Discuss their performance issues and indicate in what case one is better than the other.

5. Consider deadlocks.
   (a). What conditions will a deadlock arise? Give an example of a deadlock.
   (b). What are the methods for handling deadlocks?

6. An allocation method refers to how disk blocks are allocated for files.
   (a). What are the three typical allocation methods?
   (b). A solid-state drive (SSD) is a data storage device that uses integrated circuit assemblies as memory to store data persistently, distinguished from traditional electromechanical magnetic disk drives (HDD). Discuss the differences of block allocation between SSD and HDD.

背面尚有試題