1. Consider the amplifier shown in Fig. P1, for which $V_t$ = 1 V, $k_n'(W/L)$ = 600 μA/V², $V_{GS}$ = 3 V, $V_{DD}$ = 5 V, and $R_D$ = 2 kΩ.
   (a) Find the dc quantities $I_D$ and $V_D$. (6%)
   (b) Calculate the value of $g_m$ at the bias point. (4%)
   (c) Calculate the value of the voltage gain. (5%)
   (d) If the MOSFET has λ = 0.01V⁻¹, find $r_o$ at the bias point and calculate the voltage gain. (5%)

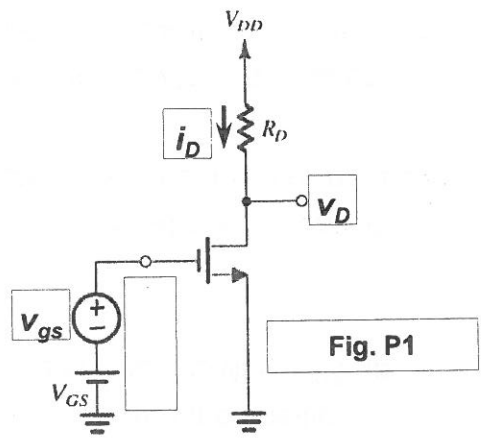

Fig. P1

2. For the NMOS amplifier shown in Fig. P2, assume the capacitances of $C_{c1}$, $C_{c2}$, and $C_s$ are infinite.
   (a) Specify the input resistance $R_{in}$ and the output resistance $R_{out}$. (8%)
   (b) Draw the high-frequency equivalent circuit of the amplifier. (4%)
   (c) Considering the internal capacitances $C_{gs}$ and $C_{gd}$, derive the high 3-dB frequency $f_H$ using Miller's theorem. (8%)

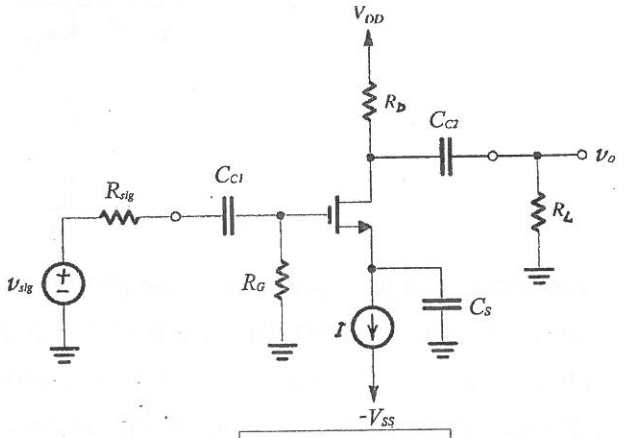

Fig. P2

3. A two-stage CMOS opamp shown in Fig. P3 is designed to provide a slew rate of 75 V/μs and a unity-gain bandwidth $f_t$ of 80 MHz.
   (a) Estimate the value of the overdrive voltage of the input-stage transistors. (3%)
   (b) If the first-stage bias current $I$ = 100 μA, find the value of $C_c$. (3%)
   (c) For a process for which $u_pC_{ox}$ = 50 μA/V², what $W/L$ ratio applies for $Q_1$ and $Q_2$? (4%)

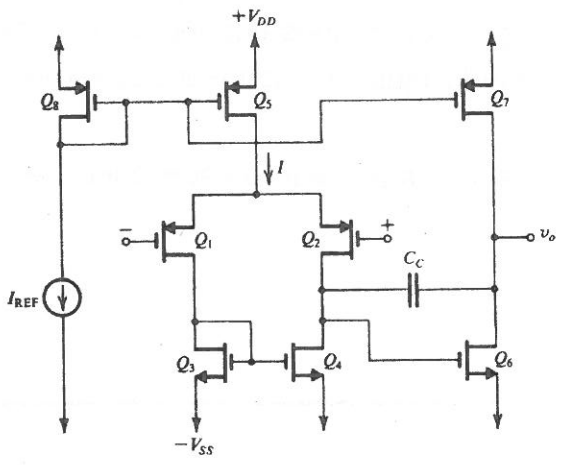

Fig. P3

4. In each of the following statements, determine whether the statement is "True (T)" or "False (F)".
   a) We can connect several diodes in series to construct a multiple input logic gate. (2%)
   b) Body effect of MOSFET will always increase the threshold voltage. (2%)
   c) A source follower is a good current buffer. (2%)
   d) The gain of a common gate amplifier can be boosted by adding a source degeneration resistor. (2%)
   e) The miller multiplication effect is observed in the common source amplifier, and reduces the bandwidth. (2%)

5. The feedback amplifier shown in Fig. P5 has two identical MOS transistors ($Q_1$ and $Q_2$) biased by ideal current sources (0.5 mA), where the overdrive voltage ($V_{OV}$), threshold voltage ($V_{th}$), and Early voltage ($V_A$) are 0.2 V, 0.5 V and 10 V for both $Q_1$ and $Q_2$. Please evaluate the gain($A_f$), input resistance ($R_{if}$) and output resistance ($R_{of}$) of this feedback amplifier. (20%)

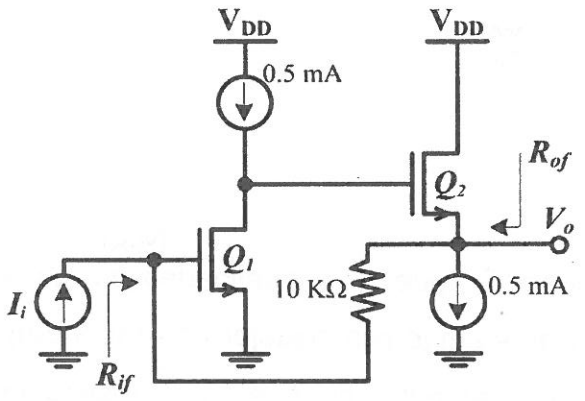


Fig. P5

6. We first design a basic matched CMOS inverter with W/L ratio of 1 μm/0.18 μm and 3 μm /0.18 μm for NMOS and PMOS, respectively. Assume the input and output parasitic capacitances of the basic matched inverter are both 4fF. Then a six input CMOS OR gate is realized in Fig. P6.
   (a) Please sketch the circuit diagram of Fig. P6. (8%)
   (b) If the transistors in (a) are sized to provide each gate with a current-driving capability equal to that of the basic matched inverter, please give the relative area of this six input OR gate and the basic matched inverter. (5%)
   (c) In case the six input OR gate is powered by 1.8 V, and has signal switching frequency of 50 MHz, and 10 MHz at nodes $N_1$($N_2$) and Y. Please estimate the power dissipation. (7%)

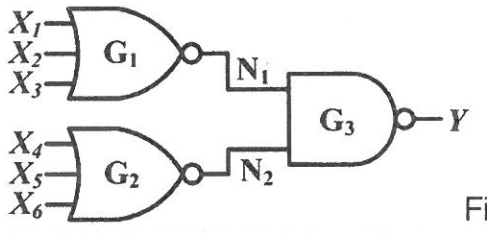


Fig. P6