國立中正大學 104 學年度碩士班招生考試試題

信號與媒體通訊組

系所別：電機工程學系-計算機工程組　　科目：計算機組織

晶片系統組

通訊工程學系-通訊乙組

第 1 節

1 (24%) Explain the following terms

1.1 (4%) Write-through vs. write-back

1.2 (4%) Virtual memory vs. physical memory

1.3 (4%) Von Neumann bottleneck

1.4 (4%) MIPS rate vs. MFLOPS rate

1.5 (4%) Memory mapped I/O vs. I/O mapped I/O

1.6 (4%) Multiprogramming

2 (12%) Booth's Algorithm and Modified Booth's Algorithm

2.1 (4%) Calculate 11101010 × 11001110 by Booth's Algorithm.

2.2 (4%) Give the rule of Modified Booth Recoding.

2.3 (4%) Find the values of P_0, P_2, P_4, and P_6 by Modified Booth's Algorithm.

multiplicand Y 11101010

multiplier X 11001110

P_0

P_2

P_4

P_6

$P = P_0 + P_2 + P_4 + P_6$

3 (14%) Carry-save (Wallace tree) multiplier

3.1 (5%) Give the architecture of 101 × 110 Wallace tree multiplier.

3.2 (9%) Give the inputs of each carry save adder.

4 (18%) The equation of Average Memory Access Time (AMAT) has three components, including hit time, miss rate, and miss penalty.

4.1 (3%) Give the equation of AMAT in terms of hit time, miss rate and miss penalty.

For each of the following cache optimizations, indicate which components of the AMAT equation can be improved. Explain the reasons.

4.2 (5%) Using a multi-level cache instead of a primary cache.

4.3 (5%) Using an *n*-way set-associate cache instead of a direct-mapped cache.

4.4 (5%) Using larger blocks instead of smaller blocks.

5 (4%) Supposing that the industry trends show that a new process technology scales capacitance by 1/2, voltage by 1/2, and clock rate by 3, by what factor does the dynamic power scale?

6 (10%) For the MIPS assembly code below,

```
        addi    $t2,    $0,     10
LOOP:   lw      $s1,    0($s0)
        add     $s2,    $s2,    $s1
        addi    $s0,    $s0,    4
        subi    $t2,    $t2,    1
        bne     $t2,    $0,     LOOP
```

6.1 (4%) What is the total number of MIPS instructions executed?

6.2 (6%) Translate the MIPS code into C code. Assume that $t2 holds the C-level integer, ***i***, $s2 holds the C-level integer, ***x***, and $s0 holds the base address of the integer array, **MemArray**.

7 (18%) Assume that a CPU datapath contains five stages with different latencies below.

IF	ID	EX	MEM	WB
300ps	400ps	350ps	500ps	100ps

7.1 (6%) What is the clock cycle time in a pipelined and a non-pipelined processor?

7.2 (6%) What is the total latency of an **add** instruction in a pipelined and a non-pipelined processor?

7.3 (6%) If we can split one stage of the pipelined datapath into two new stages for higher clock rate, and each with half the latency of the original stage, which stage would you split, and what is the new clock cycle time of the processor?