國立中山大學104學年度碩士暨碩士專班招生考試試題

科目名稱：電子學【光電所碩士班選考】　　題號：435004

※本科目依簡章規定「可以」使用計算機（廠牌、功能不拘）（問答申論題）　　

1. A PN-junction operated reversed bias exhibit I-V characteristic as illustrated in Fig. 1 (a).
   (1) Please state and explain possible mechanisms leading to such character. (10%).
   (2) When operated at the breakdown region, a diode can be used as a rectifier shown in Fig. 1(b). Please plot its equivalent circuit (4%) and find the dc line regulation $\frac{\Delta V_o}{\Delta V^+}$(4%).
   (3) $V^+ = 10V$, $R = 10k\Omega$ and $C = 100nf$. When a small signal $v_s = 0.1sin(2\pi f_s t)$ is added upon V^+, estimate the maximum frequency f_s achievable when the diode still works in breakdown region (4%) and estimate the associated phase angle between signal and output (4%).

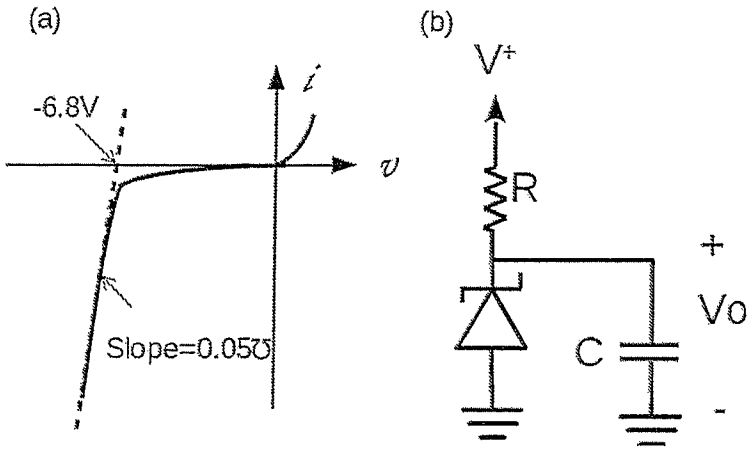

Fig. 1

2. An amplifier circuit is shown in Fig. 2 and its frequency response is given in Fig. 3. For $R_4 = 10k\Omega$, please find the values of R_1, R_2, R_3, C_1, C_2 and g_m(12%). If one insert a resistor $R_5 = 2.2k\Omega$ between node 1 and ground, what kind of feedback topology was utilized (3%)? What is the closed-loop gain $A_f \equiv \frac{V_o}{V_i}$ at zero frequency (3%)?

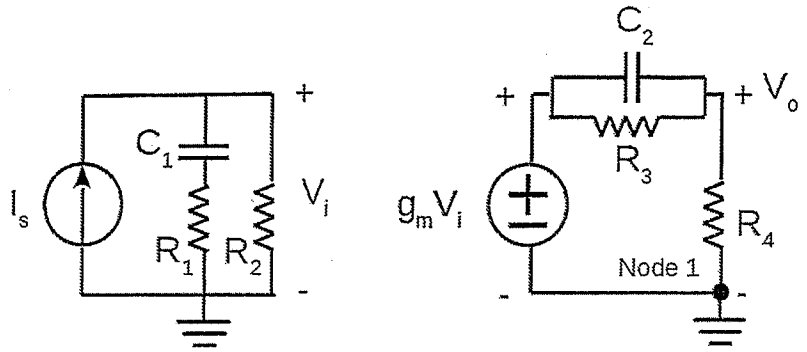

Fig. 2

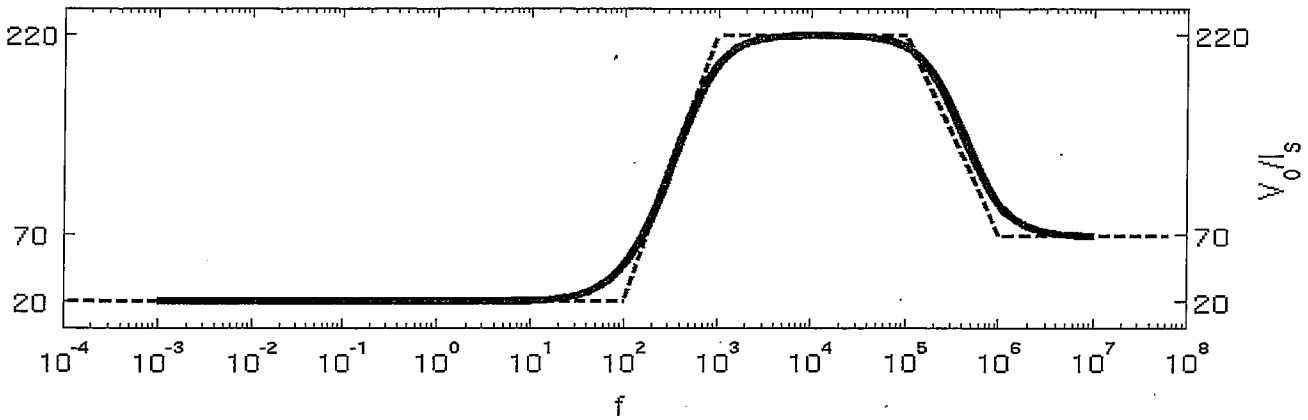

Fig. 3

3. A common-Emitter differential amplifier in Fig. 4(b) is biased by a current source built by circuit in Fig. 4(a).
   (1) Assume the current gains in Q_1 and Q_2 and are β, and in Q_3 it is β'. Obtain the expression for I_{bias}. (5%)
   (2) Assume the Early voltage of Q_3 is V_A, what is the output resistance of the current source in Fig. 4(a). (5%)
   (3) Transistors Q_1,Q_2, Q_4 and Q_5 have identical current gain β and Q_3 has its current gain β'. The Early voltage for Q_1, Q_2, Q_3 and Q_5 is V_A and Q_4 has its early voltage $(1+x)V_A$ where x is much smaller than 1. Find the expression of common mode rejection ratio (CMRR) of the CE differential amplifier in Fig. 4(b). (10%) ** credits without detailed calculation procedure.

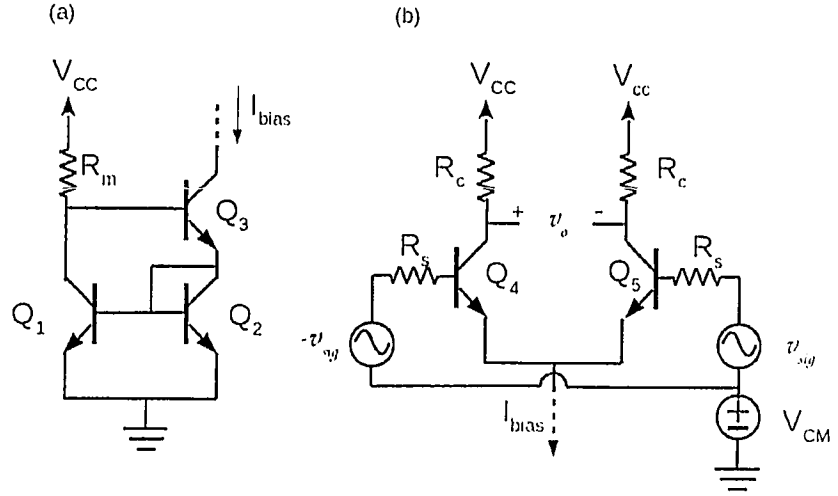

Fig. 4

4. MOSFET characteristics:
   (1) Plot the structure of n-type MOSFET. Indicate in your plot the depletion region at thermal equilibrium when drain and sources are grounded. (4%)
   (2) Explain the how depletion region is formed.(4%)
   (3) Explain the basic operations of n-type MOSFET (4%).
   (4) Explain body effect; how does it affect the device characteristics; plot the equivalent circuit model including the body effect (4%).
   (5) Explain channel length modulation and how it affect the MOSFET characteristics. (4%).
   (6) Two MOSFETs are fabricated on one substrate using the same technology. The dimension of the transistor are listed in table 1 and MOSFET are in operated in saturation region. Calculate the ratio of the following parameters: drain current (2%), channel conductance(2%), Early voltage (2%), output resistance (2%), gate-to-channel capacitance (2%) of the two transistor , i.e.

$$\frac{\text{parameteroftransistor1}}{\text{parameteroftransistor2}}$$

   (7) Explain the operation of CMOS inverters and elucidate the effect if the two transistors are not matched. (6%)

Transistor	Oxide thickness	Channel length	Channel width
#1	4 nm	0.4μm	2μm
#2	6 nm	0.8μm	8μm

Table 1