國立中山大學104學年度碩士暨碩士專班招生考試試題

科目名稱：計算機結構【電機系碩士班己組】　　題號：431005

※本科目依簡章規定「可以」使用計算機（廠牌、功能不拘）（問答申論題）　　

[Problem 1] (20%) Explain and compare the following terminology pairs.

(a) (5%) TLB (Translation Lookaside Buffer) vs Page Table

(b) (5%) Interrupt-Driven I/O vs DMA

(c) (5%) VLIW vs Superscalar

(d) (5%) Multi-Core vs Cluster

[Problem 2] (20%) Consider a four-level memory hierarchy, M1, M2, M3, and M4, with access times T1= 10 nsec, T2 = 50 nsec, T3= 100 nsec, and T4 = 600 nsec. The cache hit ratio H1 = 085 at the first level, H2 = 0.90 at the second level and H3 = 0.95 at the third level. Calculate the effective access time of this memory system.

[Problem 3] (20%) IEEE-754 floating-point representation

(a) (10%) Using 32-bit floating-point format (8-bit exponent, exponent bias = 127, and base = 2) to represent **-1/64**.

(b) (10%) Using 64-bit floating-point format (11-bit exponent, exponent bias = 1023, and base = 2) to represent **-1/32**.

[Problem 4] (20%) Consider a 32-bit microprocessor that has an on-chip 16 Kbytes four-way set associative cache. Assume that the cache has a line size of four words (each word is 32 bits).

(a) (10%) Show the 32-bit physical address (Show how many tag bits, set bits, and offset bits).

(b) (10%) Where in the cache (by indicating the set number) is the double word from memory location ABCDE8F8 mapped?

[Problem 5] (20%)A non-pipelined processor has a clock rate of 2.5 GHz and an average CPI (cycles per instruction) of 4. An upgrade to this processor introduces a new processor with five-stage pipeline. However, due to internal pipeline delays, such as latch delay, the clock rate of the new processor has to be reduced to 2 GHz and an average CPI of 1.

(a) (10%) What is the speedup achieved for a typical program with 100 instructions?

(b) (10%) What is the MIPS rate for the two processors, respectively?

<Note>: MIPS = Million Instructions per Second.